A UNIFIED POWER+CLOCK COMPILER: ENABLING RAPID IVR-IP INTEGRATION INTO ENERGY-EFFICIENT SOCS

AUTHORS: CHI-HSIANG HUANG, XUN SUN

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Motivation

Allow sophisticated, efficient SoC design with small teams

- Heterogeneous systems ➔ multiple accelerators
- Efficiency ➔ support for fine-grained V_{dd} domains
- Automated, all-digital V_{dd}, clock regulation

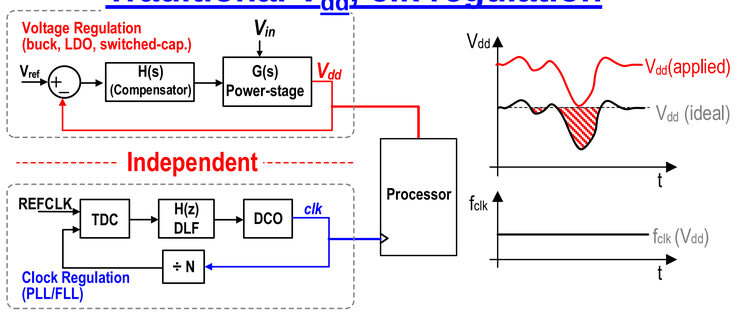
Proposed Solution: SoC domain compiler

- Input; non-V_{dd} regulated, non-clk regulated design
- Output: Physical design of all-digital V_{dd}, clk regulated design
- Automated, all-digital design flow for rapid design

Challenges

- **Fine-grained V_{dd} domains ➔ Increased V_{dd} margins**
  - Supply noise, Temp. variation

Traditional V_{dd}, clk regulation

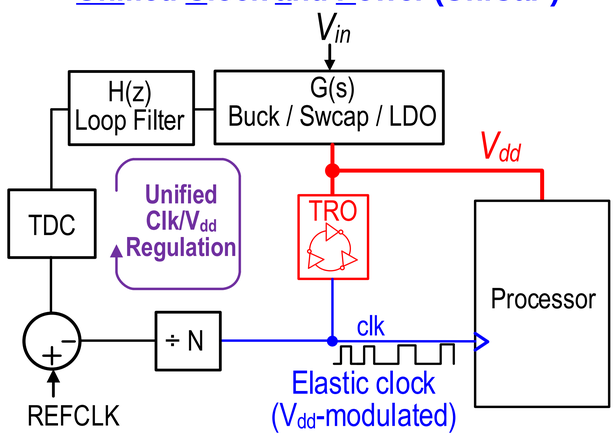


- **Drop-outs/Transient of analog LDO**
  - More than a V_{TH}-headroom voltage needed
  - Long-term design for rapid-transient response

➔ **Computational Dig. LDO**

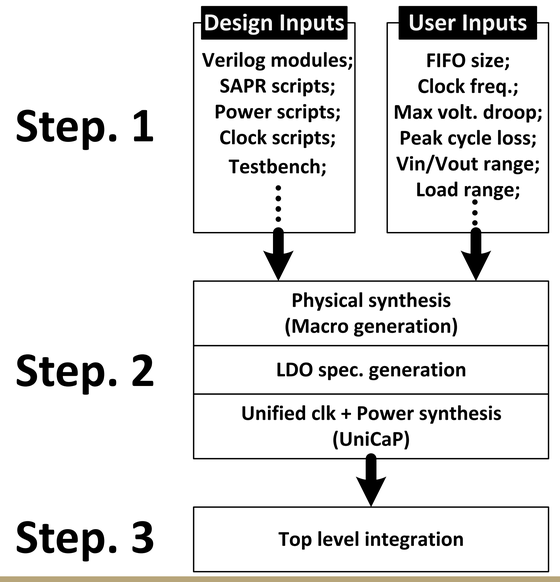
Aggressive Vdd margin recovery: UniCaP

Unified Clock and Power (UniCaP)



- **Aggressive margin ↓**
- **fclk locks to ftarget = N.fref**
- **All-digital construction ➔ Design automation**

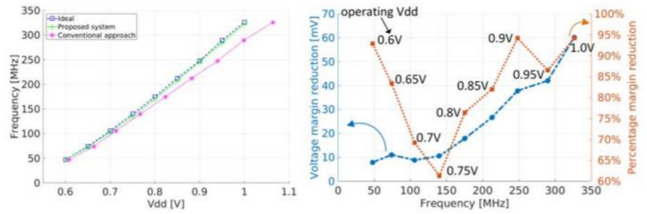
Domain synthesis flow



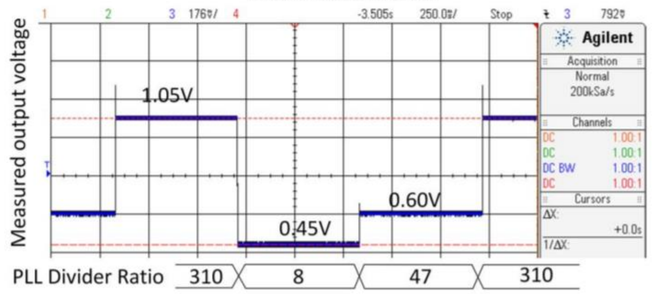
Silicon validation

Buck converter with UniCaP

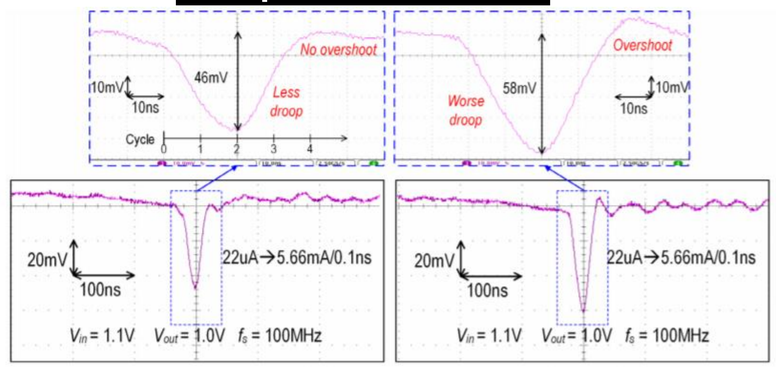
Voltage Margin Reduction



DVFS Waveform



Computational DLDO



Future Work, References, and Acknowledgments

- Build baselines for power and clock analysis
- Automatize LDO spec. and macro generation

ELECTRICAL & COMPUTER ENGINEERING
UNIVERSITY of WASHINGTON

ADVISOR: VISVESH S. SATHE