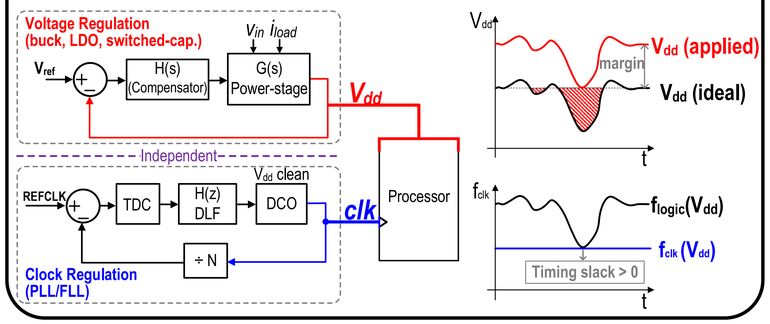
AN ALL-DIGITAL BUCK-CONVERTER-BASED UNIFIED CLOCK AND POWER ARCHITECTURE (UNICAP) WITH AUTONOMOUS CCM/DCM TRANSITION

01

STUDENTS: XUN SUN

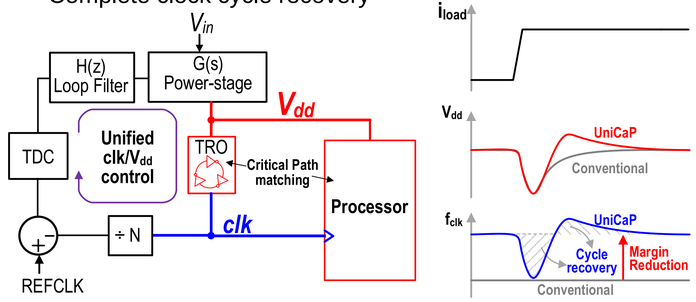
Motivation

- Independent voltage and clock regulation → **margin for worst-case** supply noise & PVT conditions.
- Dissipative margins are becoming increasingly important with IVR system and lower V_{dd}.
- Maintain high conversion efficiency across wide I_{load} range

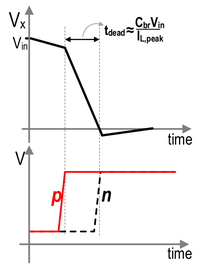


Proposed Approach

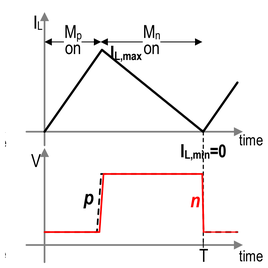
- **UniCaP** architecture
  - V_{dd}-powered Tunable Replica Oscillator (TRO)
  - Use V_{dd} control of TRO to safely maintain PLL lock
  - Complete clock cycle recovery



- **Zero-Voltage Switching (ZVS)**

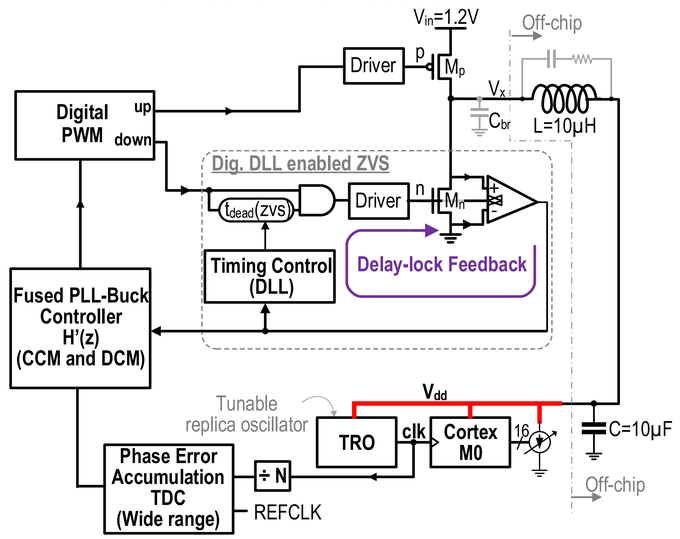


- Autonomous **CCM/DCM transition**



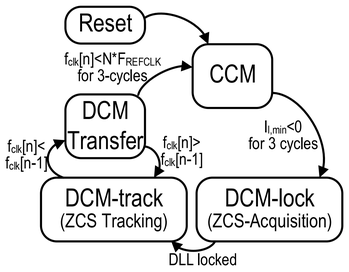
DCM mode operation

Circuit Architecture

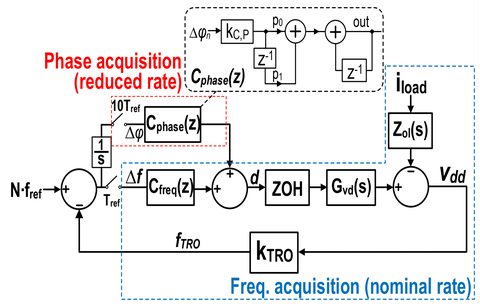


- Manage autonomous CCM/DCM transition by a Finite State Machine (FSM)
- Solve the combined PLL-buck system stability issue by employing composite control strategy

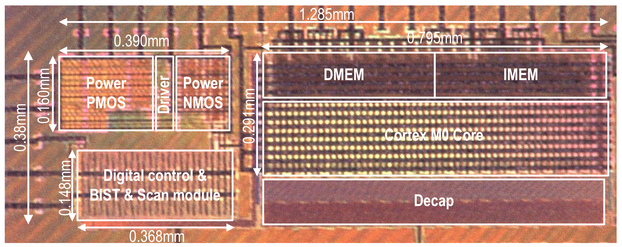
CCM/DCM FSM



Composite Control Design



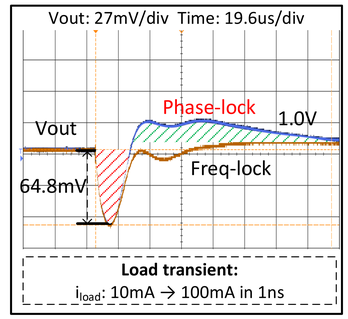
Die Photo

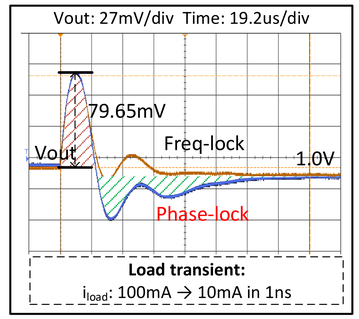


TSMC 65nm LP

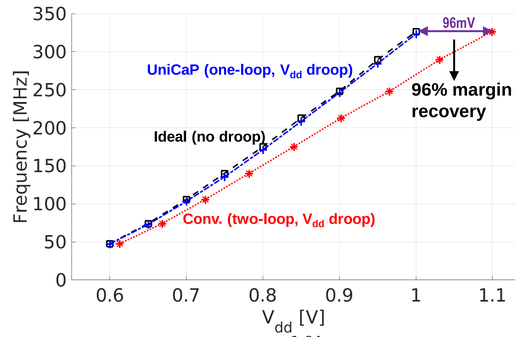
Measurement Results

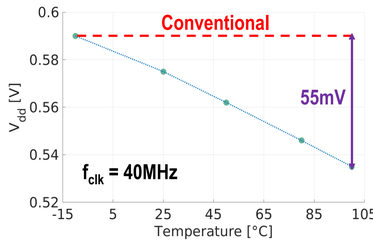
Load Transient Response

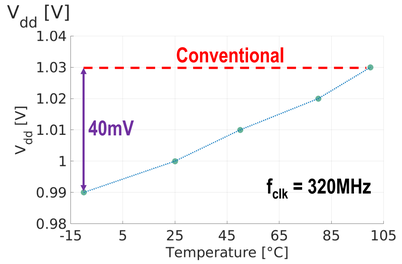




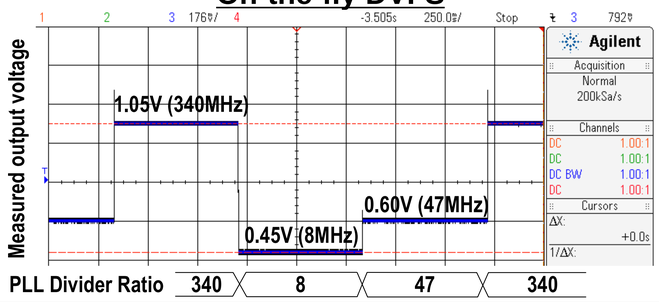
Supply Droop and Temp. Margin Reduction







On-the-fly DVFS



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SPONSORS: SEMICONDUCTOR RESEARCH CORPORATION (TASK 2712.006), INTEL & QUALCOMM