

INTEGRATING BIDIRECTIONAL BRAIN-COMPUTER INTERFACES IN LOW-VOLTAGE CMOS STUDENT: JOHN UEHLIN

treatment of neurophysiological disorders.



triggered FES C. Moritz, S. Perlmutter, E. Fetz;







- High-power stimulation distorts nearby recordings.

ELECTRICAL & COMPUTER ENGINEERING

UNIVERSITY of WASHINGTON

ADVISORS: JACQUES C. RUDELL, VISVESH SATHE SPONSORS: MEDTRONIC, NSF CENTER FOR NEUROTECHNOLOGY

equal

- underlying recording data.



the sensitive recording input.



- 65nm CMOS Test Chip Includes:
 - 4-Channel 12V, 2mA Max STIM
 - 64-Channel 2kS/s Recording
 - Real-time Adaptive Digital Artifact Cancellation

- Productize test chip for use in research labs.

Stimulus Artifact Cancellation

• Stimulation energy jams connected recording systems.

• Large (10mV), prolonged (10ms) voltage artifacts obscure

• Using the recording (SENSE) output, on-chip digital learns the artifact shape through iterative voltage subtraction at

Fully Integrated Bidirectional Interface in 65nm CMOS

H-Bridge 5	H-Bridgei
Stim 1	Stim 2
H-Bridge	H-Bridger
Stim 3	Stim 4
	Artifact
Time Multiplexed	Canceller
Recording	Memory & DSP

Future Work

• Integrate circuit ideas in future Medtronic products. • Published in ESSCIRC 2019 and to appear in JSSC 2020.