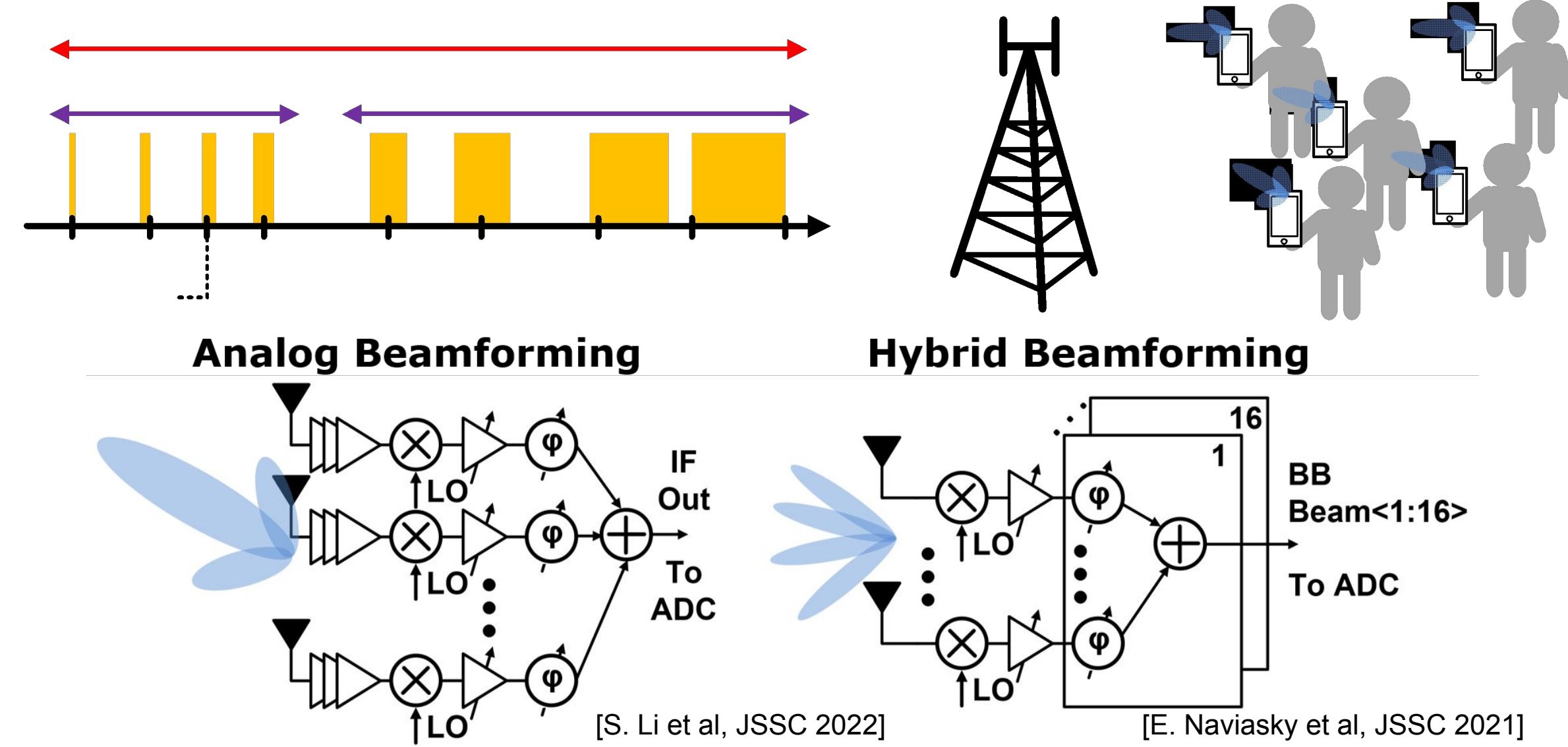




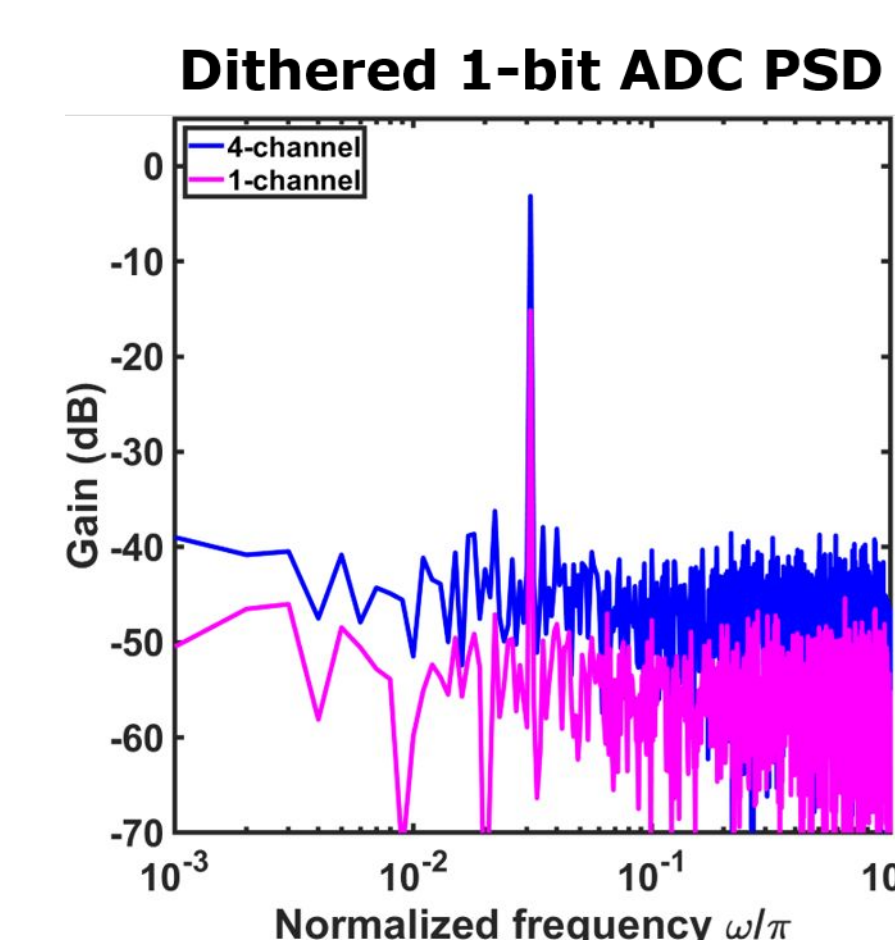
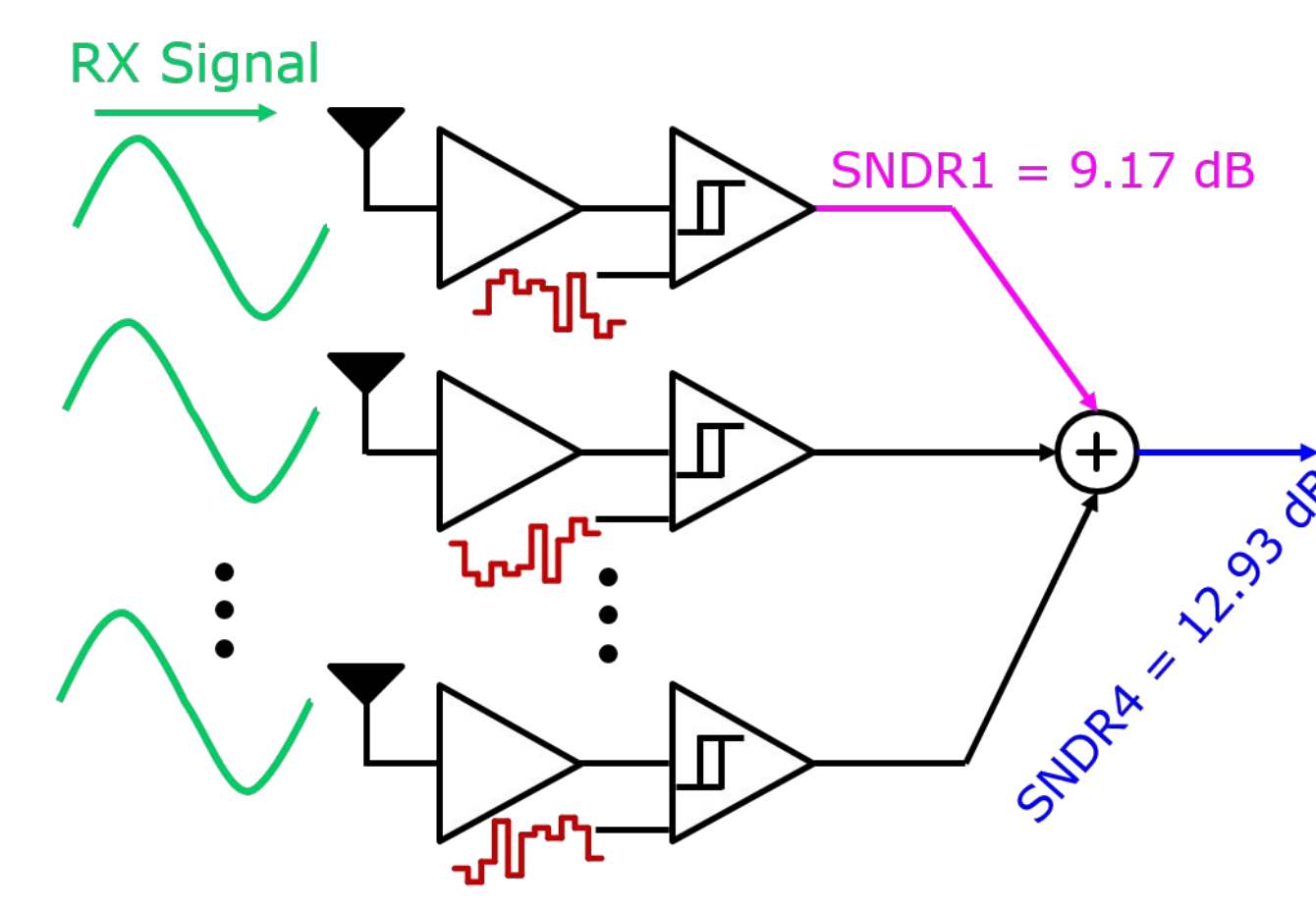
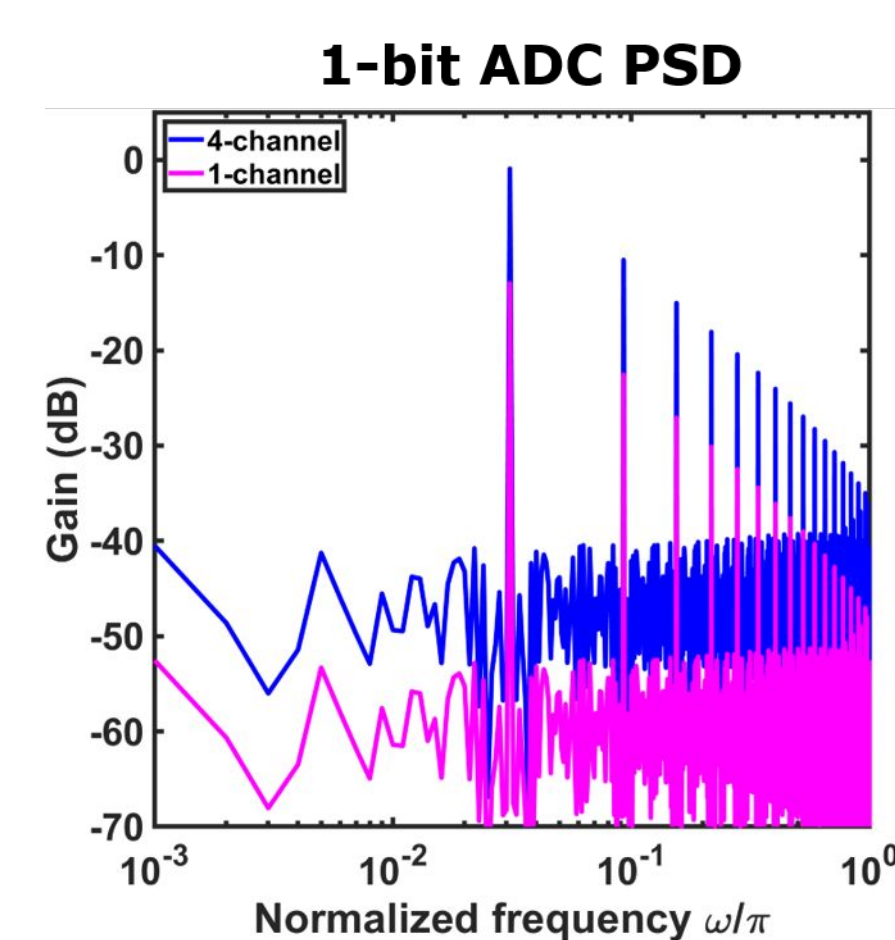
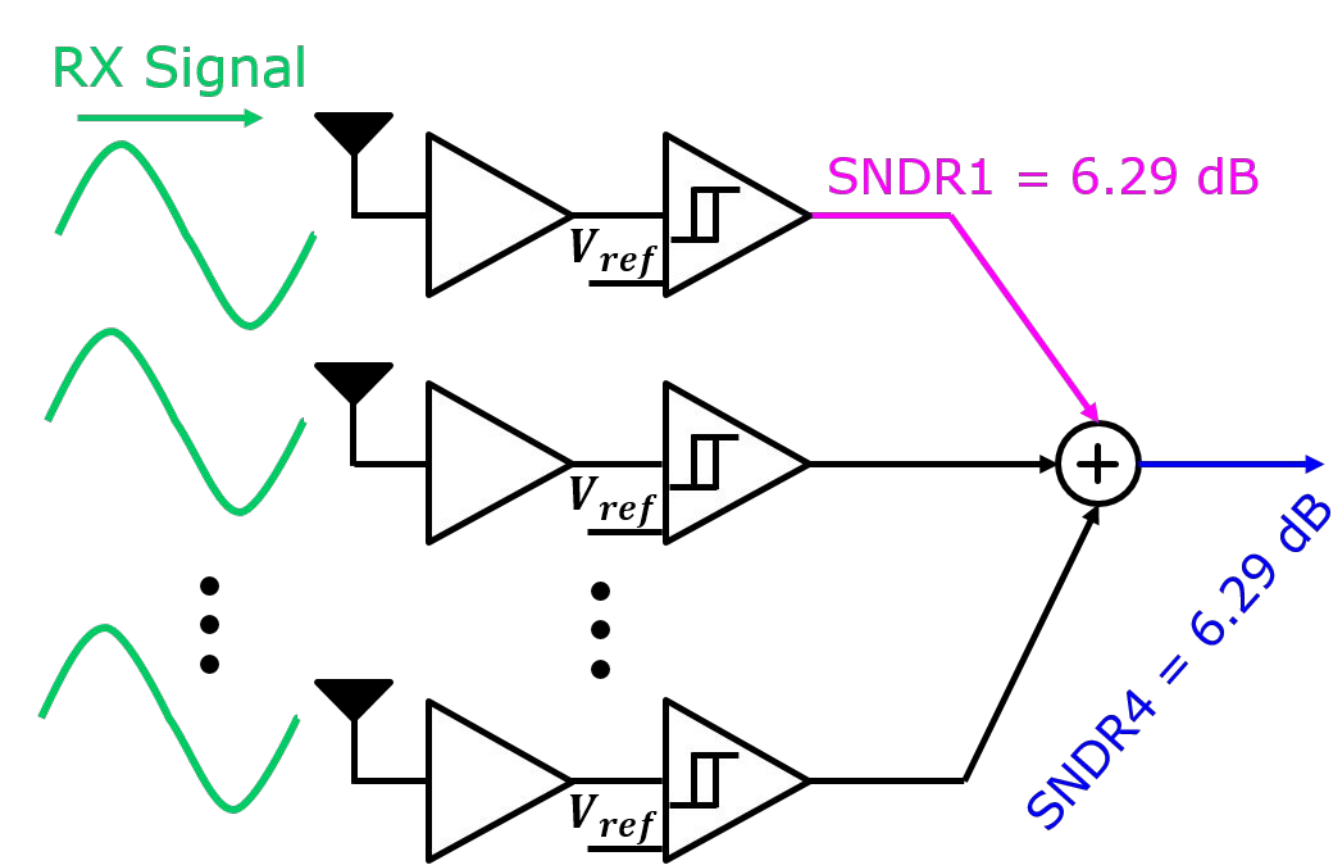
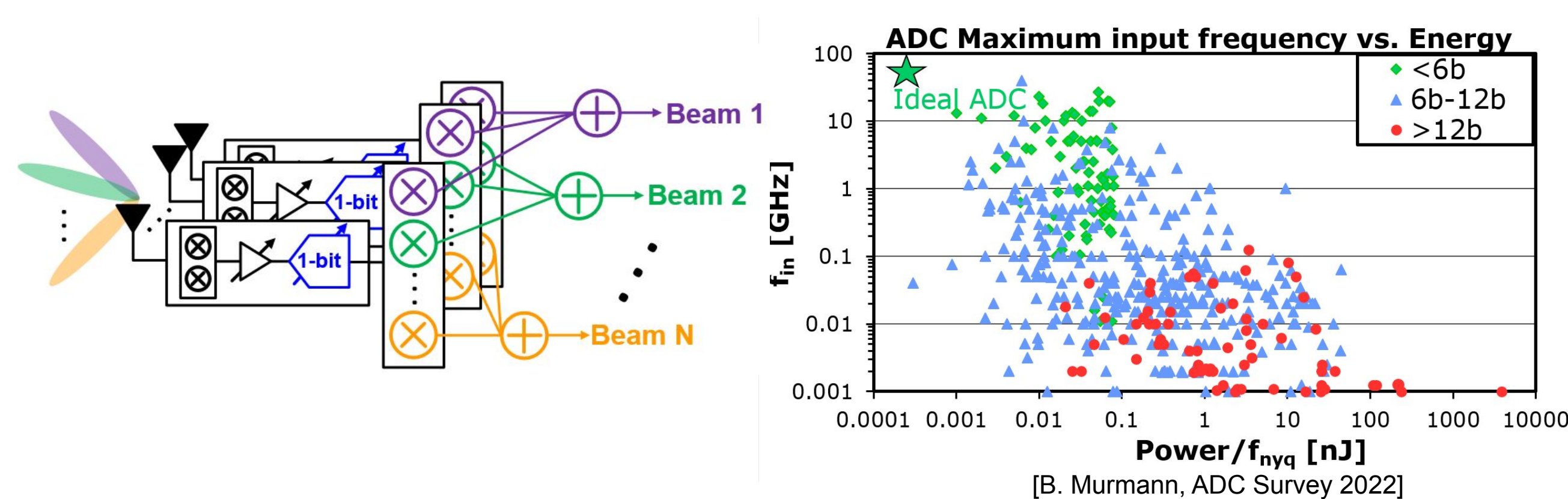
A Millimeter-Wave Digital Beamforming Receiver using Low-Resolution ADCs

STUDENTS: DENIZ DOSLUOGLU

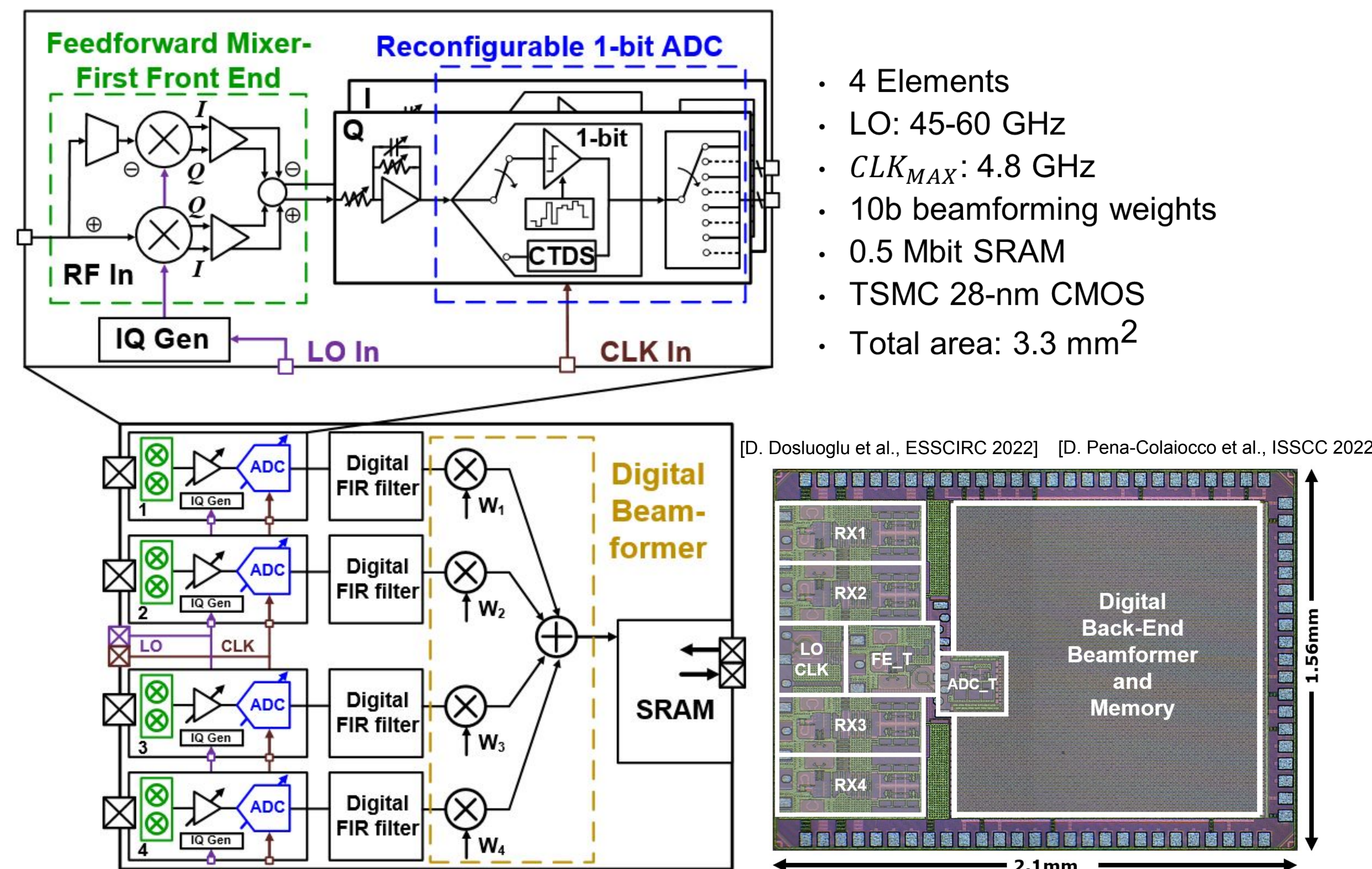
Millimeter-Wave Receivers for 5G



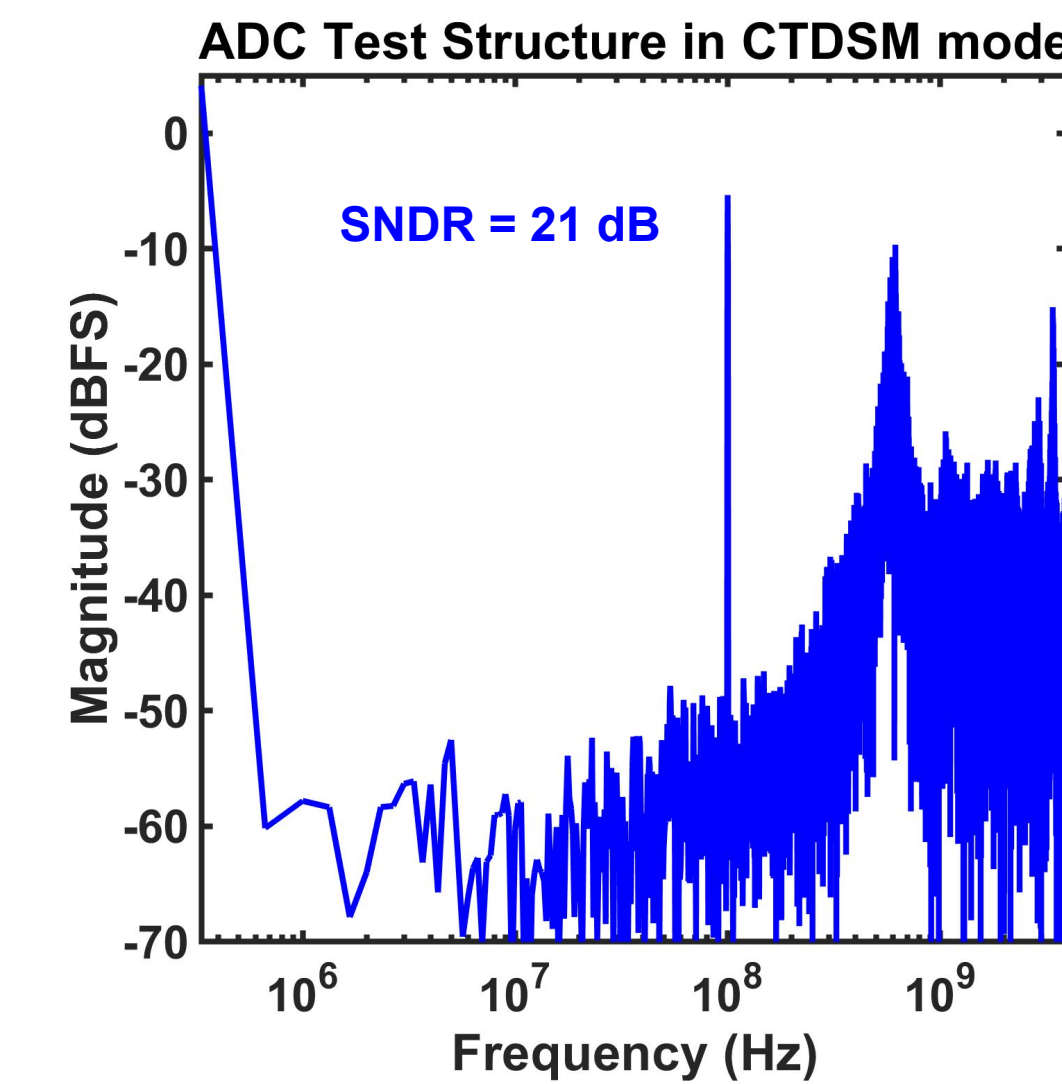
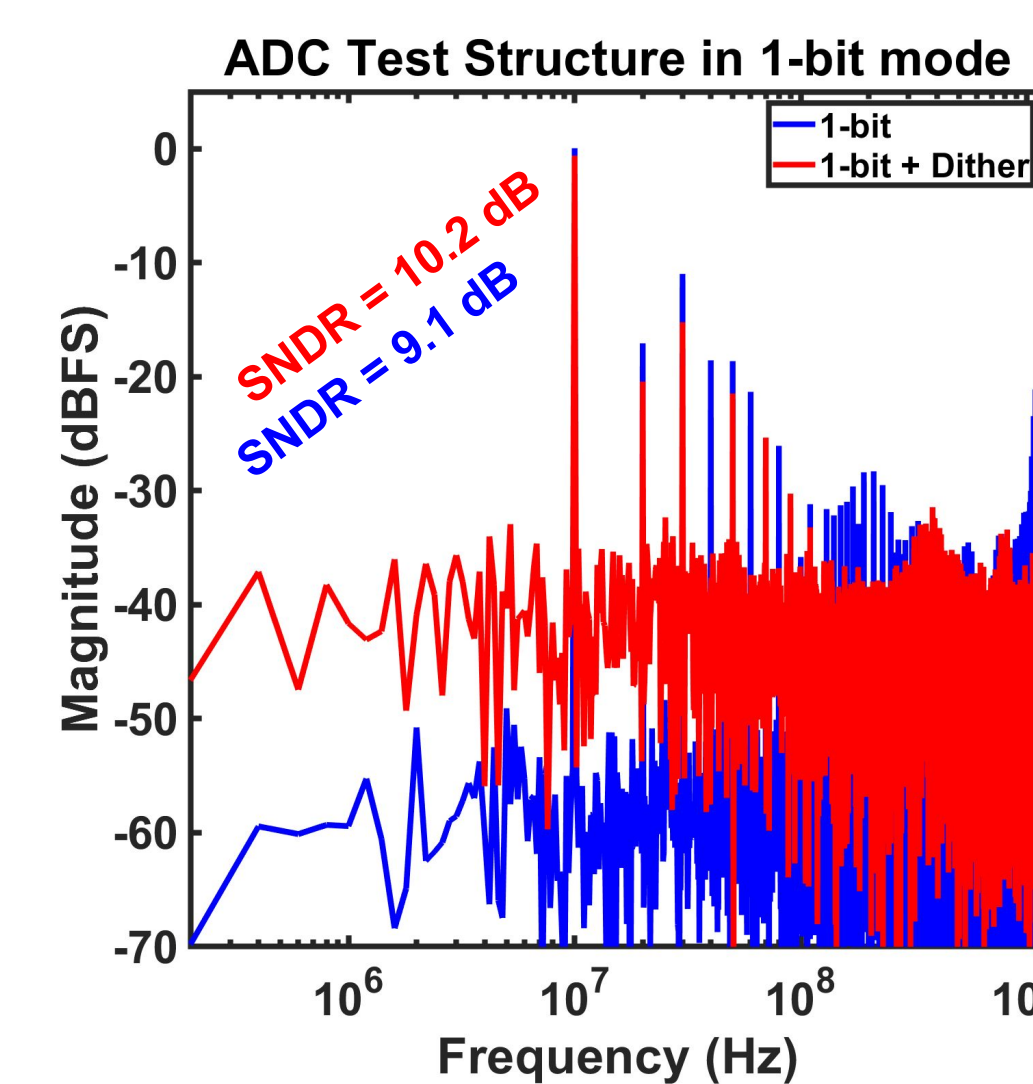
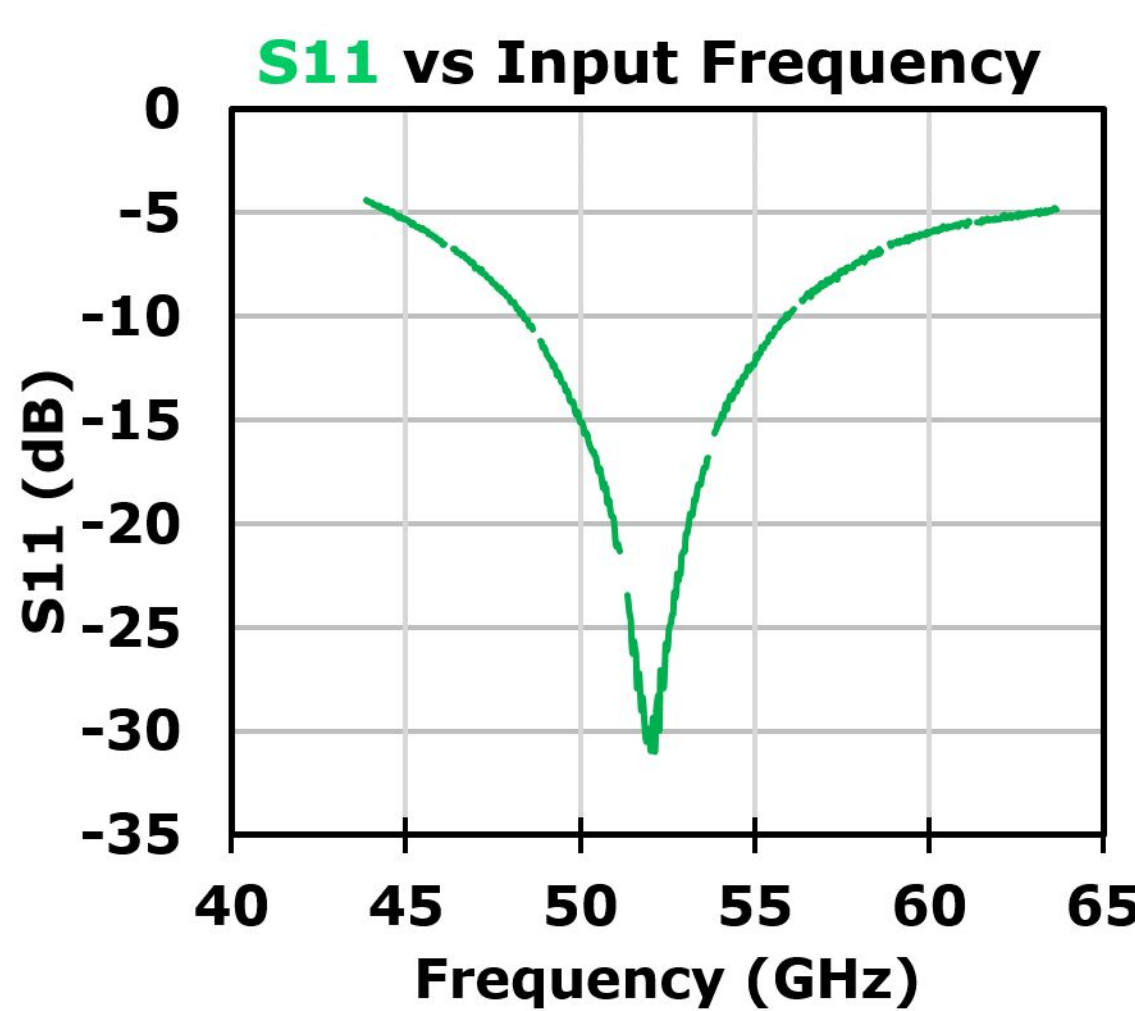
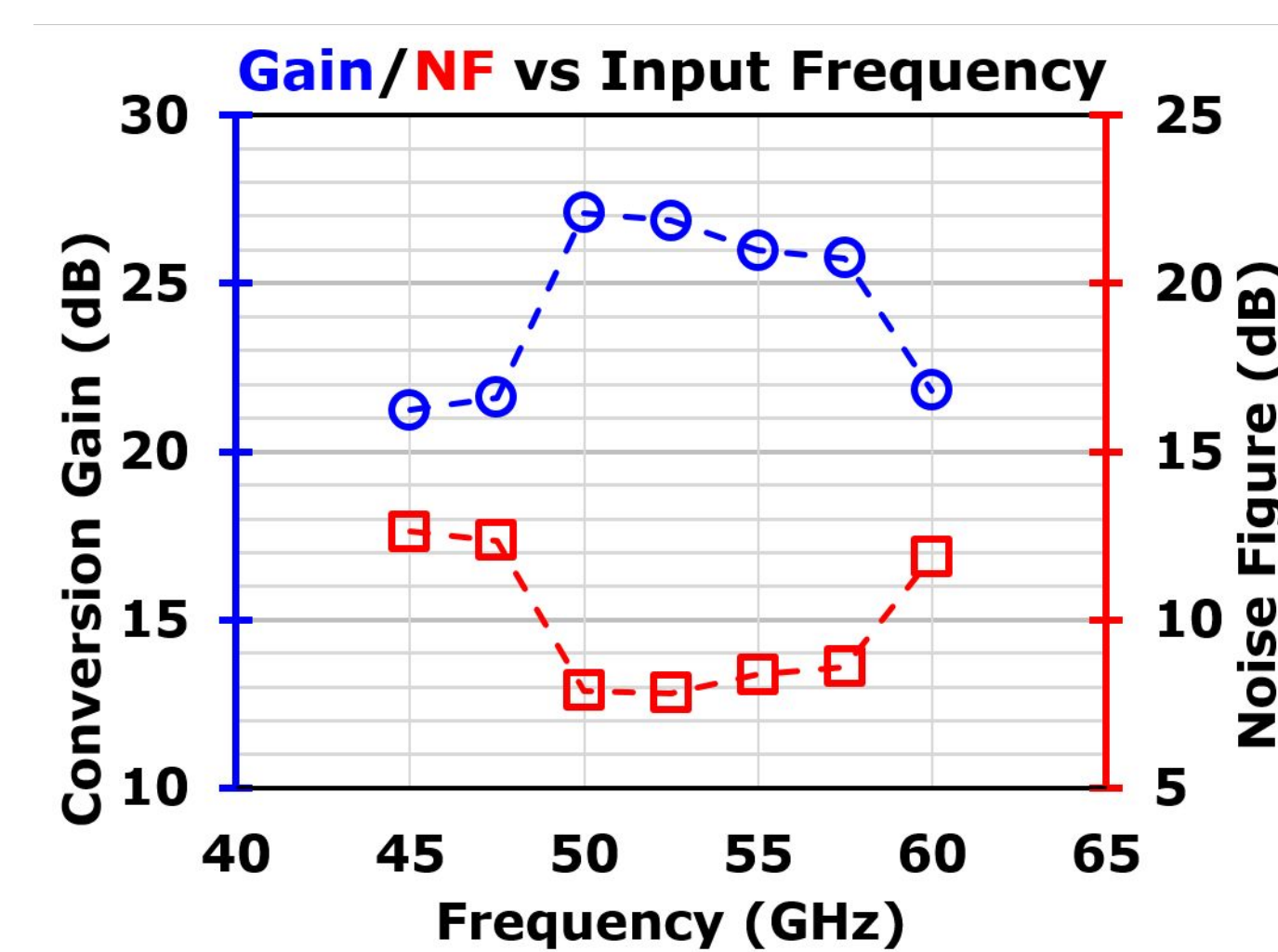
Digital Beamforming with Low-Resolution ADCs



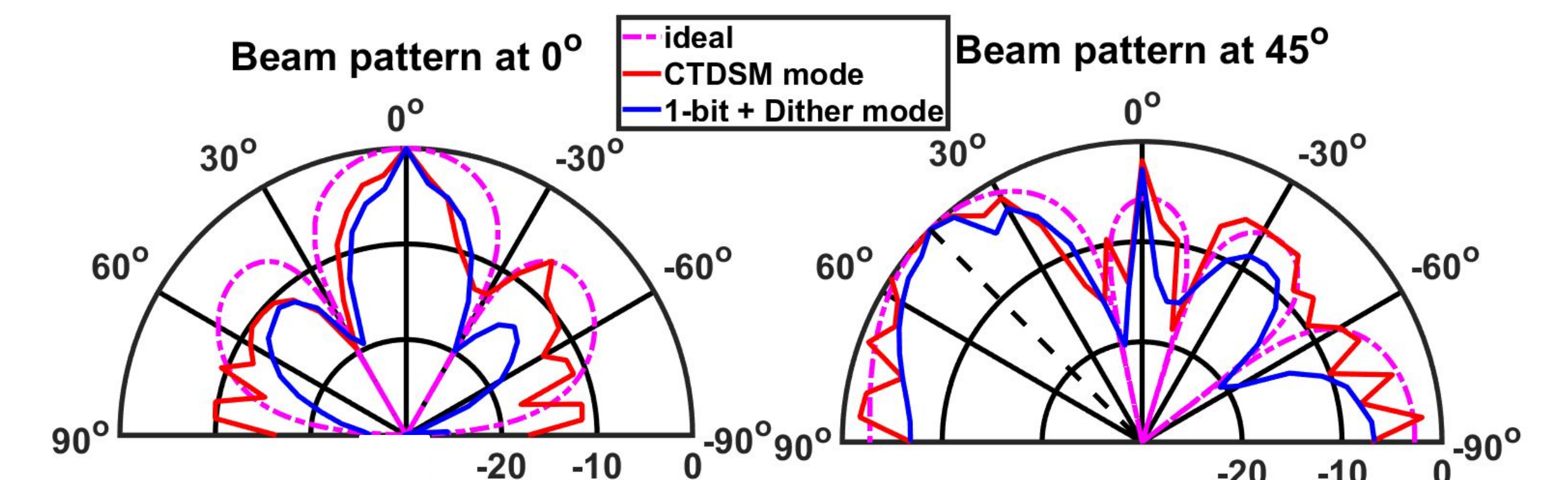
Prototype Chip



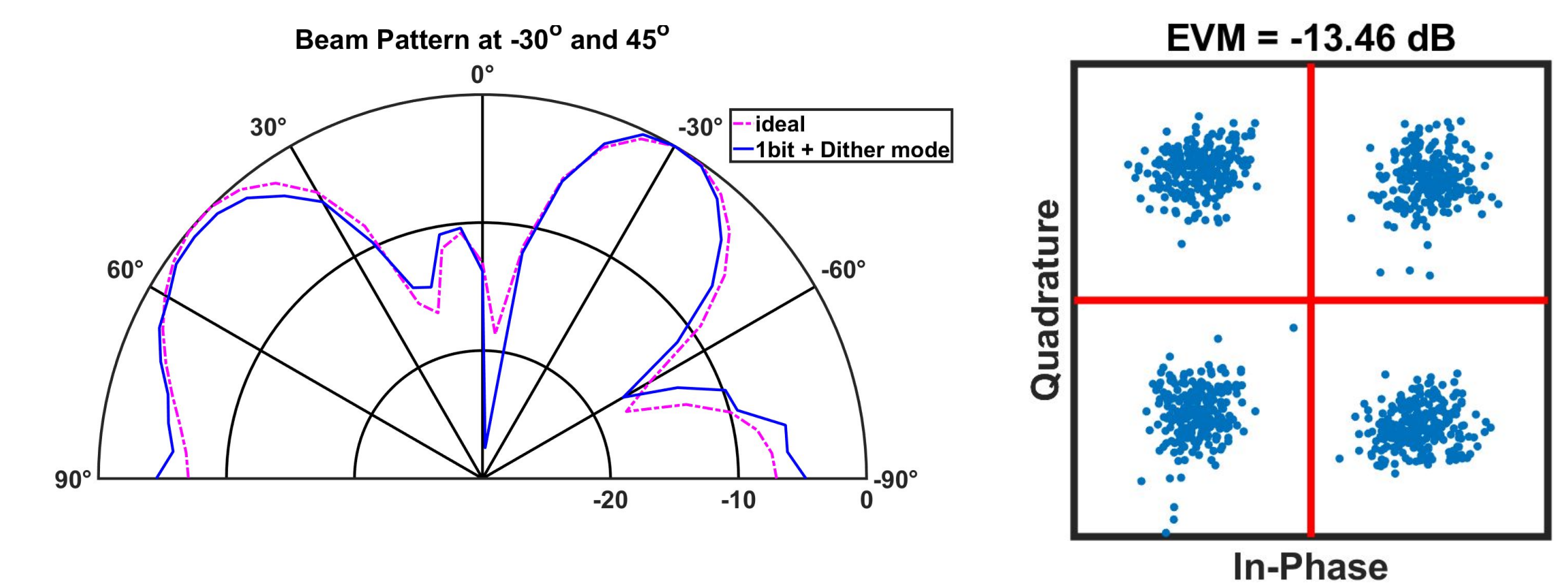
RF Front-End and ADC Test-Structure Measurements



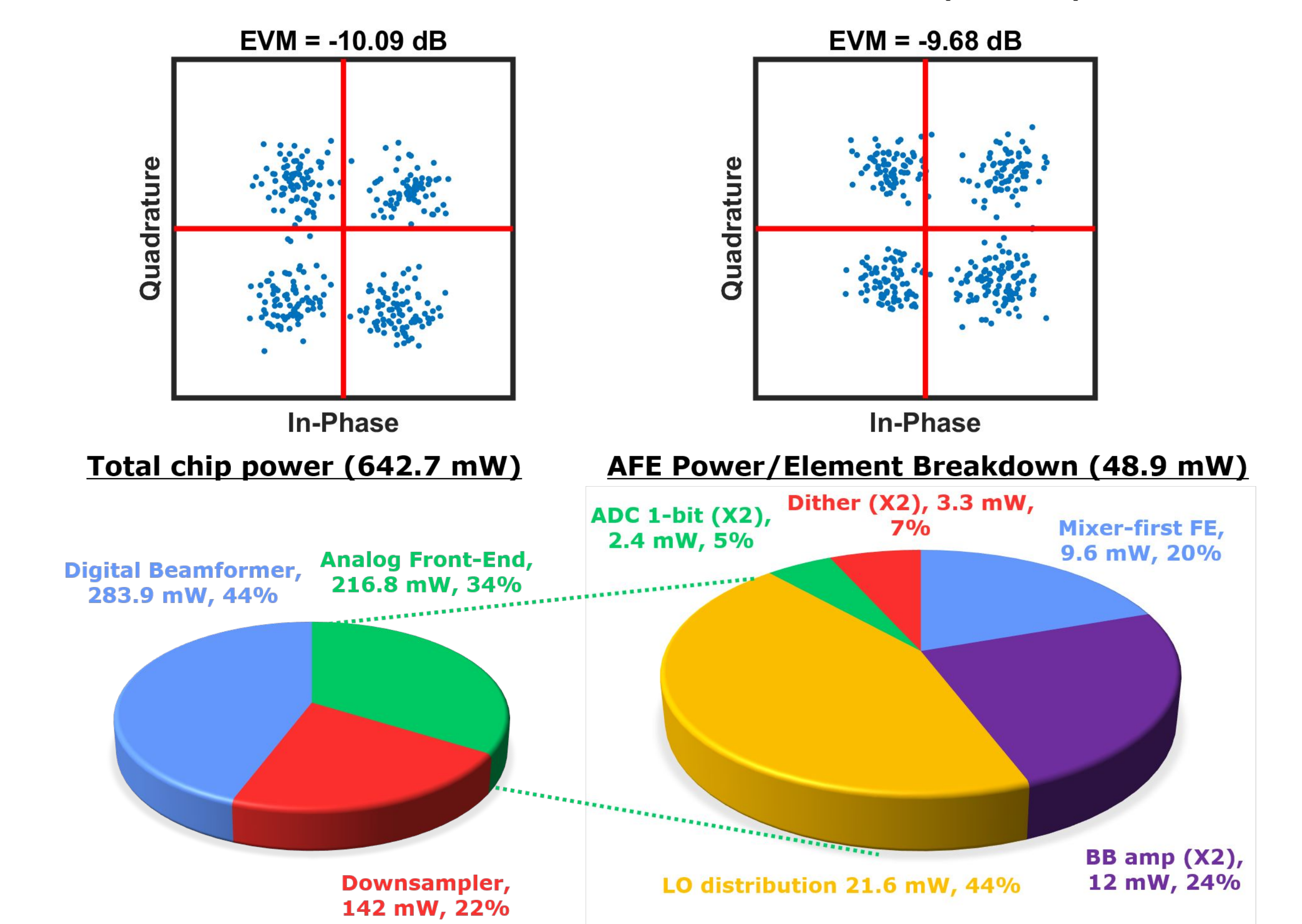
System-Level Measurements



Dithered 1-bit ADC 1-beam 400 MS/s



Dithered 1-bit ADC 2-beam 333 MS/s (0°, 30°)



- S. Li et al., "An Eight-Element 140-GHz Wafer-Scale IF Beamforming Phased-Array Receiver With 64-QAM Operation in CMOS RFSOI," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 57, no. 2, pp. 385-399, Feb. 2022.
- E. Naviasky et al. A 71-to-86-GHz 16-Element by 16-Beam Multi-User Beamforming Integrated Receiver Sub-Array for Massive MIMO. *IEEE JSSC*, 56(12):3811-3826, 2021.
- B. Murmann, *ADC Performance Survey 1997-2021*, [online] Available: <https://web.stanford.edu/~murmann/adcsurvey.html>.
- D. Dostluoglu et al. "A Reconfigurable Digital Beamforming V-Band Phased-Array Receiver," *ESSCIRC 2022- IEEE 48th European Solid State Circuits Conference (ESSCIRC)*, Milan, Italy, 2022, pp. 493-496.
- D. Pena-Colaiocco et al. "An Optimal Digital Beamformer for mm-Wave Phased Arrays with 660MHz Instantaneous Bandwidth in 28nm CMOS," *IEEE International Solid-State Circuits Conf (ISSCC)*, 2022.