A STUDY ON THZ PLASMONICS IN A CMOS CONTINUUM TRANSISTOR ARRAY

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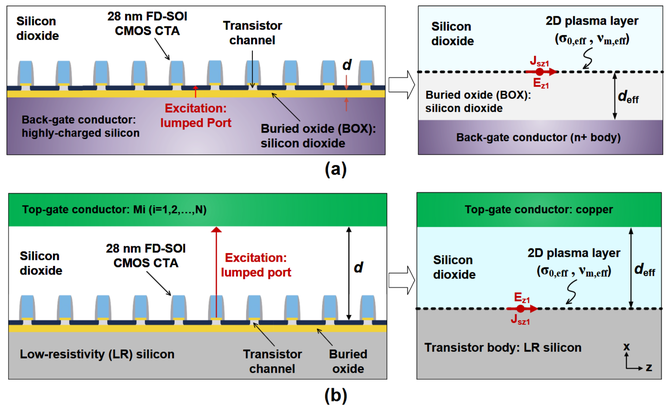
Design Motivations

- Overcome CMOS limitations at THz frequencies by addressing charge transit time and parasitic capacitances that restrict f_{max} and reduces current handling.
- Explore plasma wave amplification in CMOS transistors as a novel approach to enable THz signal amplification.
- Develop a theoretical and simulation framework using a hydrodynamic transport model and Pierce's theory to analyze plasma wave propagation in a 28 nm FD-SOI CMOS continuum transistor array (CTA).
- Design and fabricate a 700 GHz plasma wave amplifier to demonstrate practical THz signal amplification along the plasma wave propagation path.

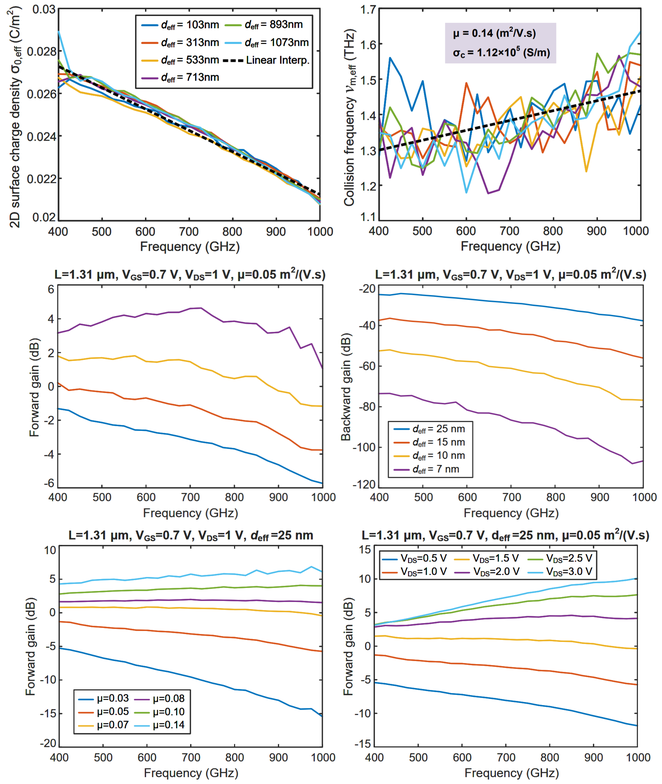
Theory

- **Gated Plasma Wave Behavior:** Understanding the operation of the Continuum Transistor Array (CTA) requires analyzing plasma wave behavior in back-gated and top-gated topologies while distinguishing gate conductors from transistor gate contacts.
- **2D Plasma Layer Model:** The CTA is represented as a 2D plasma layer characterized by effective surface charge density and charge collision frequency, with key distance parameters linking individual transistor properties to the equivalent plasma system.
- **Plasma Wave Dynamics:** Plasma waves, analogous to space-charge waves in microwave tubes, are governed by the equations of motion, continuity, and Maxwell's equations, revealing how energy from the DC electron stream is transferred to plasma waves.



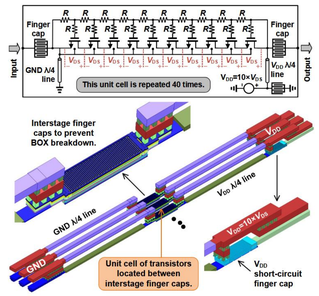
Simulation Analysis

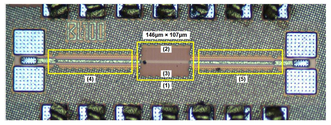
- **Application of Transcendental Equations:** The established equations for gated plasma waves are applied to model a Continuum Transistor Array (CTA).
- **Simplification Using the Drude Model:**
  When no DC current is present $V_{DS} = 0$, the Drude model is used instead of the hydrodynamic transport model.
- This allows for HFSS simulations of the transistor array, where the DC conductivity is defined as $\sigma_c = \frac{q\rho_0}{\nu_m m^*}$
- **Condition for Validity:**
  The simplification holds when the DC drift velocity v_{beam} is much smaller than the plasma wave velocity.
  The extracted parameters under zero DC current, $(\sigma_{0,eff}, \nu_{m,eff})$ remain applicable even when $V_{DS} \neq 0$.
- **Equivalent 2D Plasma Layer Representation:**
  The transistor array is replaced with an equivalent 2D plasma layer.
  Key parameters—plasma wavenumber k_z, $\sigma_{0,eff}$, $\nu_{m,eff}$ and d_{eff} are extracted from HFSS modeling.

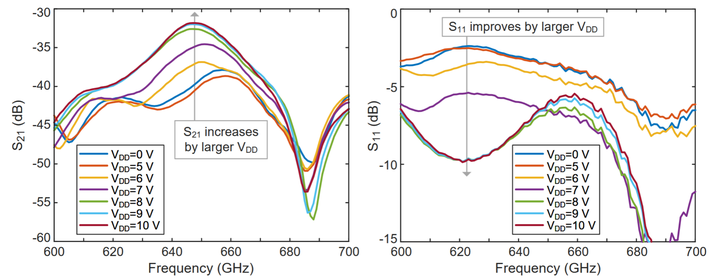


Experiment

- A back-gated plasma wave amplifier (PWA) was designed and fabricated for 700 GHz operation. It uses ten transistors, uniformly biased for stable V_{GS} and V_{DS}.
- **Biasing strategy:**
  - Kilo-ohm resistors and quarter-wave lines at V_{DD} and GND to prevent THz energy loss.
  - Large interstage finger capacitors are used to isolate CTA groups and prevent substrate and BOX breakdown.
  - Up to 10V can be applied across each CTA.
- **Array Configuration:**
  - Forty unit cells are cascaded to achieve sufficient gain.
  - The fabricated chip has a total area of 0.31 mm^2 (including pads).
  - The measured DC power consumption is 1.29 W.







Ref.	Active layer (AL)	L (μm)[a]	distance (nm)[b]	SWS	E-field (V/mm)	Gain (dB/mm	Frequency
[6]	n-GaAs (AL)	2000	1000	Dielectic	120	0.4	10 GHz
[5]	GaAs/AlGaAs	2600	∼450	Dielectic	15	0.8	76.5 GHz
[4]	GaN/AlGaN	8.3	∼30	Metallic	964	21.8	75-110 GHz
This work	28nm FDSOI CMOS	1.3[c]	25	None	7,600[d]	62[e]	650 GHz

Future Work

- Re-simulate behavior using Sentaurus or COMSOL replacing the Drude Model equations with those of the Hydrodynamic Model
- Exploring different transistor configurations such as GaAs and GaN as these alternatives are expected to enhance mobilities, with potential to achieve a positive net gain.

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