A 5-GHZ PHASE-LOCKED LOOP USING OVER-SAMPLING FEEDFORWARD PHASE NOISE CANCELLATION

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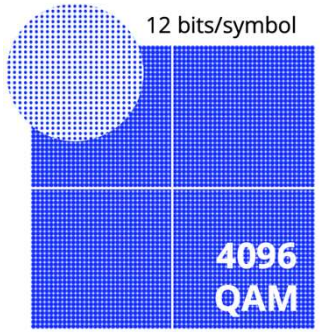
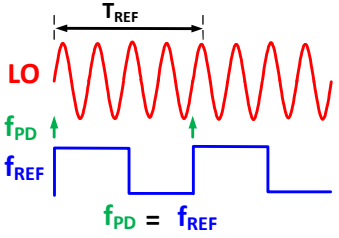
Demands for Low-Jitter Sub-6GHz PLL



Wi-Fi 7 (IEEE 802.11be):

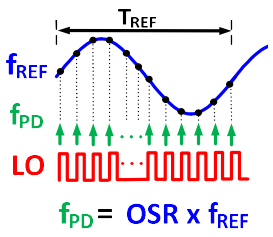
- Phase noise of LO causes the constellation diagram to rotate. → EVM degradation
- Stringent jitter requirement for the required EVM for high-order modulation schemes
- Ultra-low RMS jitter (~140 fs) is required for 4K-QAM

Concept of Over-Sampling FFPNC PLLs



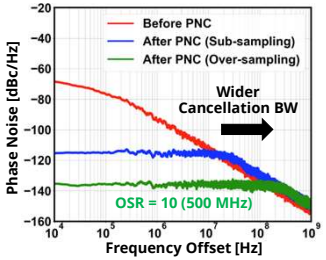
Sub-sampling PD:

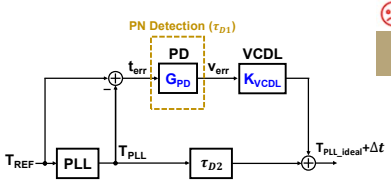
❑ Detect the phase error every reference cycle.



Over-sampling PD:

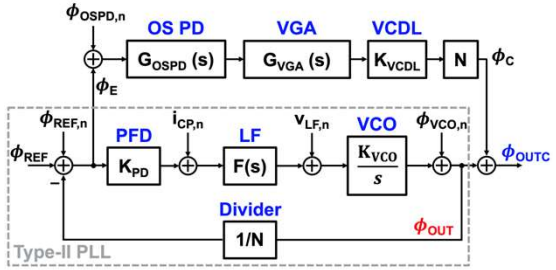
❑ Detect the phase error every PLL cycle. → More frequent detection in one reference period.





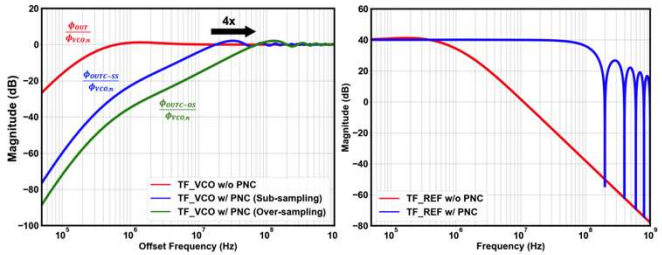
- Jittery PLL_{OUT} leads to voltage deviations in the sampled data
- Convert the voltage deviations back into the phase error
- Realign the phase of the PLL_{OUT} by Voltage-Controlled Delay Line
- Break the trade-off between the loop bandwidth and PNC bandwidth

Phase Domain System Block Diagram



$$G_{OSPD}(j\omega) = K_{OSPD} \cdot e^{-j\pi\frac{\omega}{OSR\cdot\omega_{REF}}} \cdot \frac{\sin\left(\frac{\pi\omega}{OSR\cdot\omega_{REF}}\right)}{\frac{\pi\omega}{OSR\cdot\omega_{REF}}}$$

$$G_{CAN}(j\omega) = G_{OSPD}(j\omega)\cdot G_{VGA}(j\omega)\cdot K_{VCDL}\cdot N$$



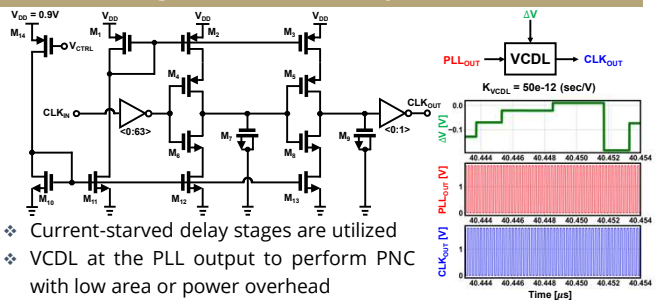
$$\frac{\phi_{OUT}(j\omega)}{\phi_{VCO,n}(j\omega)} = \frac{1}{1+OL(j\omega)} \qquad \frac{\phi_{OUT}(j\omega)}{\phi_{REF,n}(j\omega)} = \frac{OL(j\omega)\cdot N}{1+OL(j\omega)}$$

$$\frac{\phi_{OUTC}(j\omega)}{\phi_{VCO,n}(j\omega)} = \frac{1}{1+OL(j\omega)}\left(1-\frac{G_{CAN}(j\omega)}{N}\right) \qquad \frac{\phi_{OUTC}(j\omega)}{\phi_{REF,n}(j\omega)} = \frac{\phi_{OUT}(j\omega)}{\phi_{REF,n}(j\omega)} + \frac{G_{CAN}(j\omega)}{1+OL(j\omega)}$$

☺ VCO noise is suppressed by an additional factor

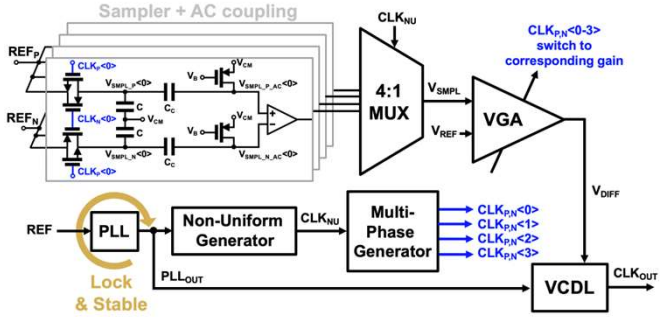
☹ REF noise directly passes to the ϕ_{OUTC} through the auxiliary path

Voltage-Controlled Delay Line (VCDL)



- Current-starved delay stages are utilized
- VCDL at the PLL output to perform PNC with low area or power overhead

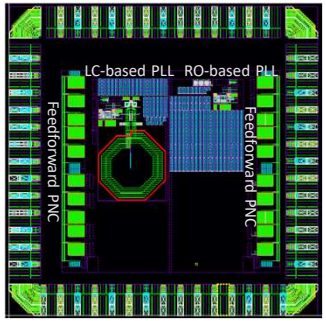
Proposed Over-Sampling PNC Architecture



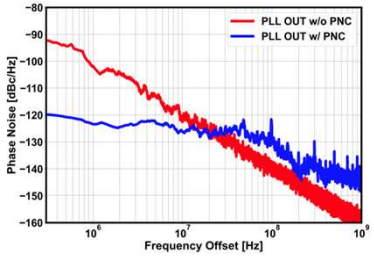
- OSR = 4

Future Plan

- ✓ **Two Type-II PLLs with different VCOs (LC-based and RO-based).**
- ✓ **Feedforward phase noise cancellation path on each PLL.**
- ✓ **TSMC 28nm CMOS process.**



Simulation Results and Conclusions



Type II Ring-VCO-Based PLL:

- f_{REF}/ f_{PLL} = 50 MHz/ 5 GHz
- PLL loop BW = 500 KHz
- Attain ~20MHz cancellation BW
- RMS jitter = 188 fs
- Phase noise = -123 dBc/Hz at a 1-MHz offset

- ✓ **Inherently stable**
- ✓ **Wide-band PNC with a low-frequency REF clock**
- ✓ **Capable of being applied to different frequency bands**

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