SAR ADC for Mobile Wireless Communication

STUDENTS: Kiet Tran, Jordan Wu, Daikun Wu, Bryan Kim, Holle Lam

ADC for Mobile Wireless Communication

- Communication data rates improve every year. The most advanced Wi-Fi protocol - Wi-Fi 7 - has a theoretical throughput of 23 Gbit/s.
- SAR ADC with digital-friendly architecture also scales due to Moore's Law.
- Key challenges: power efficiency, linearity, speed, area constraints, noise

System Definition

Specifications	Target/Expected
Supply Voltage	1.8 V
Effective Number of Bits (ENOB*)	> 8 bits
Sampling Rate	> 40 MS/s
SINADR **	> 49.92 dB
Input range	0.455 - 1.345 V
Power Consumption$_{non\text{-}ideal}$ ***	< 2.5 mW

Wi-Fi 802.11 ac protocol inspired!

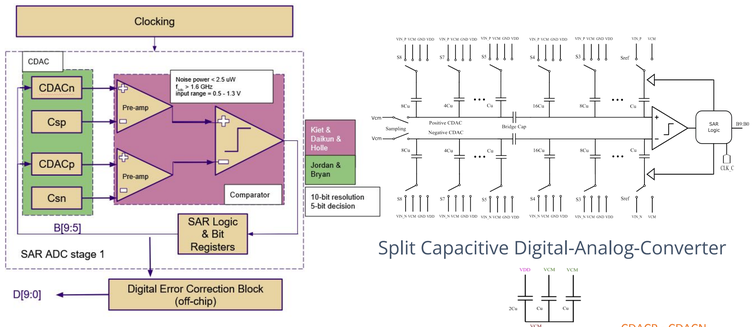
Note:

•* ENOB = (SDNR - 1.76) / 6.02

•** SQNR = 10*log(P_{Signal}/P_{Noise})

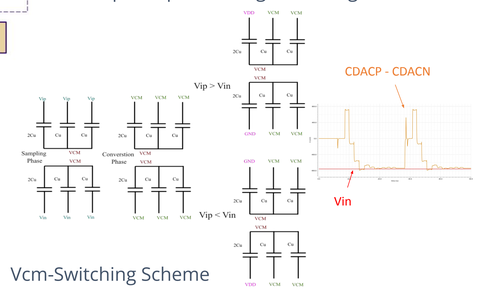
•*** $P_{non\text{-}ideal}$ is obtained by finding the "headroom" noise allowed after accounting for quantization error between 10 bits and our target 8 bits and the errors caused by offsets.

System Architecture



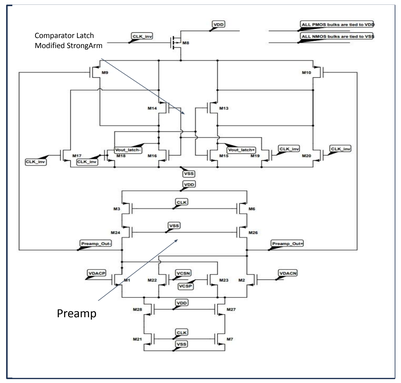
System Block Diagram

Split Capacitive Digital-Analog-Converter

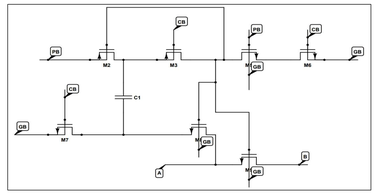


Vcm-Switching Scheme

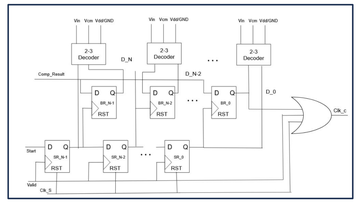
Circuit Design & Topology



Comparator Schematic

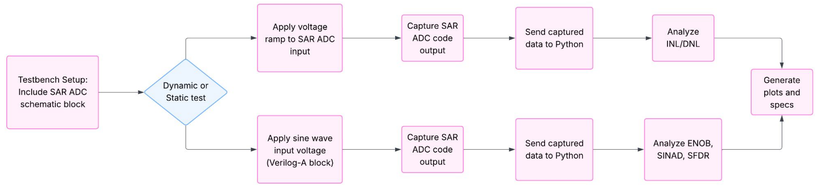


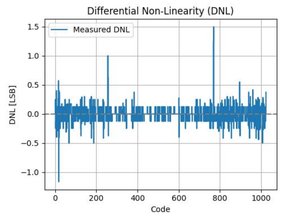
Bootstrap Switch

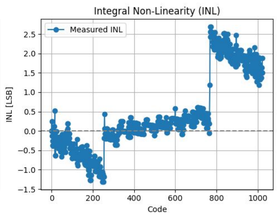


Sar Logic Digital Block

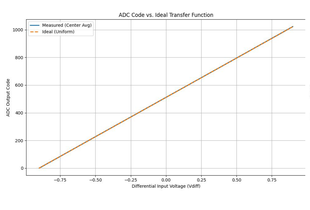
Customized and Reusable Testbenches & Verification

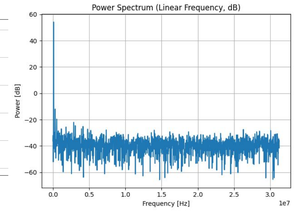




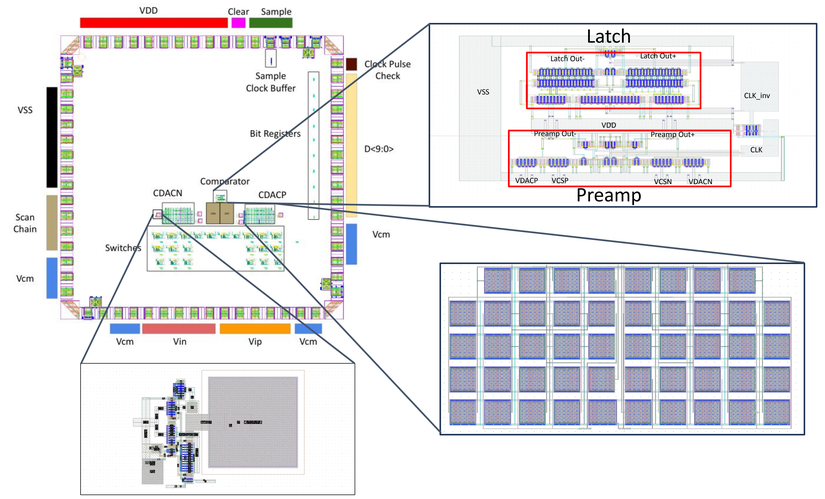


- Schematic Simulation Result
  - Transfer Function (left)
  - Digitized Input Spectral Power (right)
  - DNL (left)
  - INL (right)





Layout & Floorplan



Simulation Results

Specifications	Schematic Results	Layout Results
Effective Number of Bits (ENOB*)	9.44	6.58
Sampling Rate	66.67 MS/s	47.6 MS/s
SINADR **	58.6 dB	41.38 dB
Input range	0.45 - 1.35 V	0.45 - 1.35 V

Next Steps, References, and Acknowledgements

- Top Level Layout and Routing
- Optimize the trade-offs between the CDAC parasitic mismatches and system's non-linearity.

Faculty: Jacques C. Rudell
TAs: Elpida Karapepera, Ahmed Aboulsaad, Xichen Li

[1] Baker, R.. (2010). CMOS: Circuit Design, Layout, and Simulation, Third Edition. 10.1002/9780470891179.
[2] Y. Zhu et al., "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1111–1121, Jun. 2010, doi: 10.1109/JSSC.2010.2048498.

ELECTRICAL & COMPUTER ENGINEERING
UNIVERSITY of WASHINGTON

ADVISERS: Jacques C. Rudell

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