LINEARIZED N-PATH FILTER CHIP DESIGN FOR MIXER FIRST RECEIVER

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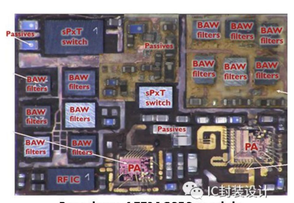
Motivation

- For today's communication system, a good transceiver or receiver should be able to implement both High-Q Filtering and Reconfigurability.
- Current solutions are SAW and BAW filters, whose resonant frequency is fixed.
- This makes them bulky, expensive and power inefficient. (Front End of 5G low band from Broadcom)

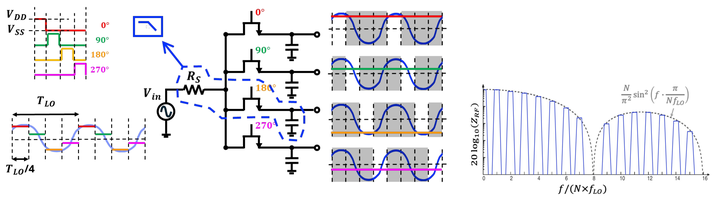


Broadcom AFEM 8050 module

- As CMOS technology has improved a lot, N-path filters offer a compact, low power, and tunable alternative compared to traditional SAW or BAW filters.

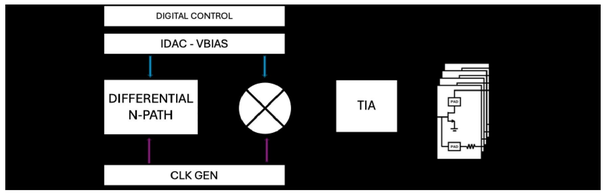
N-Path Filter

- $f_{in} = f_{LO} = f_C$
- The input signal is upconverted to $2f_C$ and downconverted to BB.
- R_s and switch resistance implement as LPF with the capacitor.
- Filtering the mixed input signal to BB.
- The output voltage is equal to the average of the input signal that each capacitor samples during the phase that it is on.



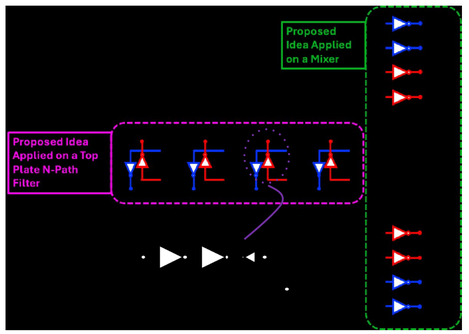
System Definition

- Differential RF signals will be converted to four BB signals by the 4-path filter.
- The BB signal will be upconverted to RF again by the mixer.
- Two N-path filters and mixers are put on this chip for tape-out:
  (a) our proposed design with a feedback (FB) topology,
  (b) a simpler structure without FB.
- Both share the same overall system architecture.

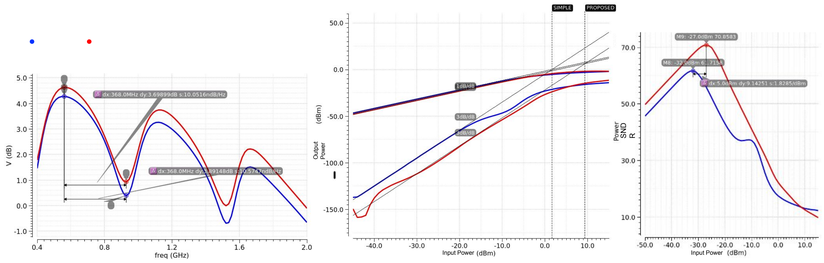


Proposed Design of N-Path Filter

- Although N-path filters looks charming so far, they are facing linearity issue due to unideal switching behavior.
- $r_{on} = \frac{V_{DS}}{I_{DS}} \approx \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS}-V_{TH}-\frac{1}{2}V_{DS}\right)}$
- We want to keep r_{on} constant. E.g. For an ideal switch, the value is 0.
- We want to add a scaled V_{DS} to V_{GS} to keep $(V_{GS} - V_{TH} - \frac{1}{2}V_{DS})$ constant.
- Feedback voltage is applied to the gates of the switches through a weaker inverter for both N-path filter and mixer.

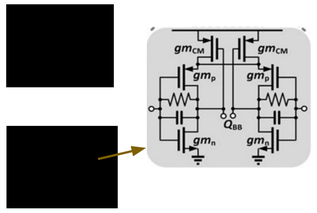


- This N-Path filter is designed using TSMC 180nm process, working at 500 MHz.
- We compared the rejection, IIP3, and SFDR of the proposed four-path filter (with FB) and a simple four-path filter (without FB), as shown below.
- Same rejection ability, but IIP3 and SFDR increased by 7.9 dB and 9.1 dB respectively.



Transimpedance Amplifier [1]

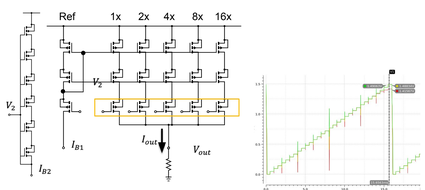
- The BB TIA simultaneously provides a low-ohmic termination of the mixer, 1st order channel filtering and I-V conversion of the BB RF current.
- Inverter based TIA offers low noise and good power efficiency.
- Here, PMOSs on the top provide low CM gain, while maintaining the high differential gain.
- This topology reduces the power consumption and noise compared to adding an extra CMFB circuit.
- We added digital controlled capacitors and resistors for higher tunability, to compensate the linearity after tape out.



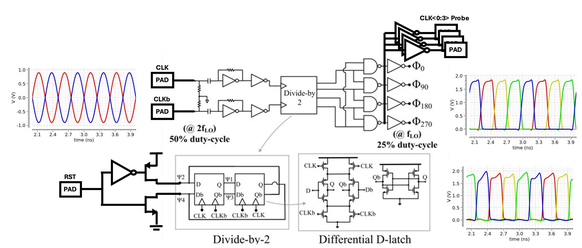
Clock and Bias Generation Circuitry

- Based on simulation results, the gate biasing voltage should be able to be tuned between 0 to 1.2 V.

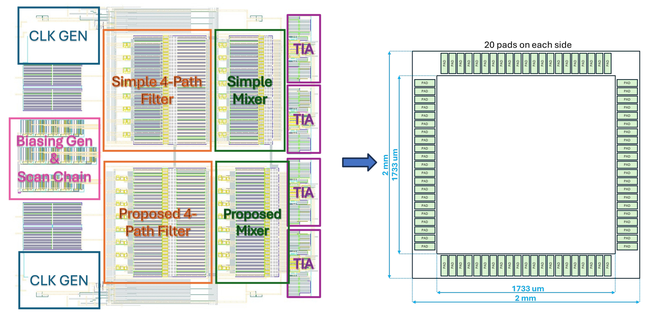
SPECS FOR CURRENT DAC	
FS I_{out}	25 uA
Resolution	5 bits
LSB	806 nA
Output Compliance Volt	0 – 1.5 V



- 4-phase clock generation [2].
- 25% duty-cycle w/o overlapping.



Floorplans and Layout



Future Work, References, and Acknowledgments

- Tape out on 6/18.
- Testing plan for the chip.
- PCB design for chip measurement.

Thanks to:
Faculty: Jacques "Chris" Rudell
PhD Students: Xichen Li, Ahmed Aboulsaad

[1] Y. Lien, E. Klumperink, B. Tenbroek, J. Strange and B. Nauta, "24.3 A high-linearity CMOS receiver achieving +44dBm IIP3 and +13dBm B1dB for SAW-less LTE radio," 2017 IEEE ISSCC, San Francisco, CA, USA, 2017, pp. 412-413, doi: 10.1109/ISSCC.2017.7870436.
[2] V. K. Purushothaman, E. A. M. Klumperink, B. T. Clavera and B. Nauta, "A Fully Passive RF Front End With 13-dB Gain Exploiting Implicit Capacitive Stacking in a Bottom-Plate N-Path Filter/Mixer," in IEEE JSSC.

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