CMOS Circulator and Qubit State Reader for Monolithic Quantum Control

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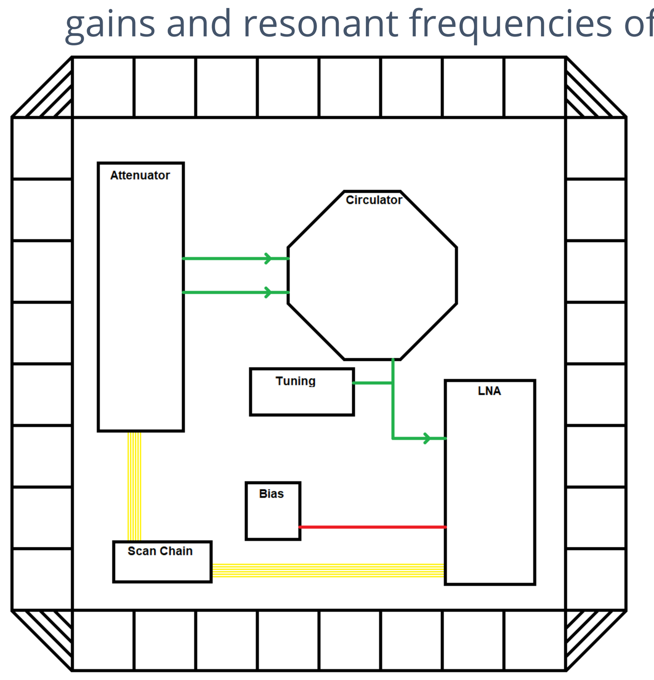
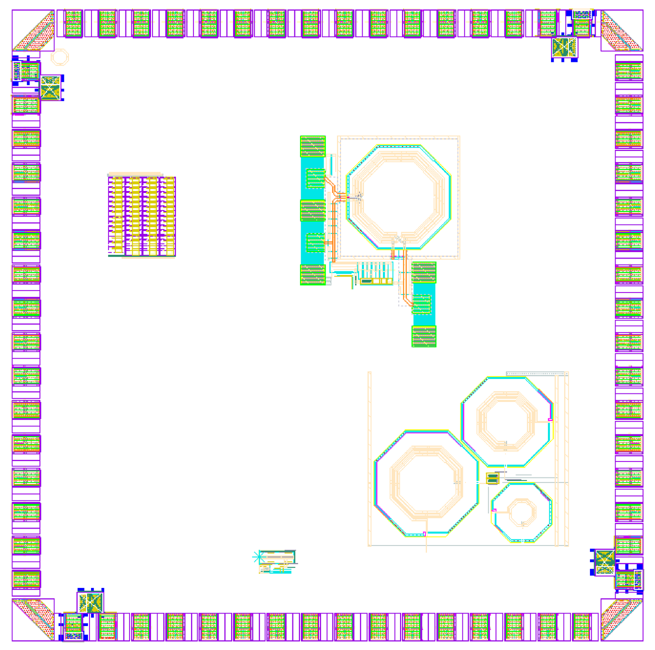
Background and Motivation

The current state-of-the-art systems for quantum computing rely on large, rack-mounted devices for qubit control, demanding two cables per qubit. It is estimated that a useful quantum computer will need hundreds to thousands of qubits, so this interconnect requirement must be reduced. Moving the control circuitry onto a single chip addresses this issue. This work aims to bring monolithic quantum computing closer to reality by integrating the circulator, a 3-port RF component that routes signals into and out of an antenna with low cross-talk, onto the same silicon as the control logic. If successful, this work will bring scalable and portable quantum computing closer to fruition.

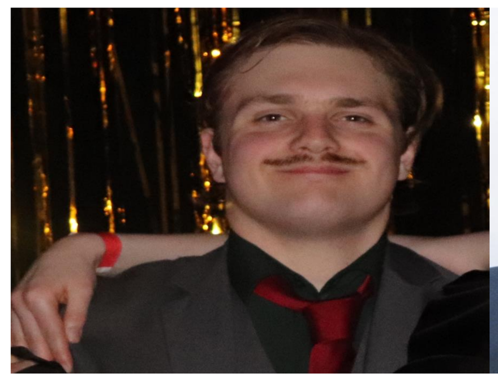
Integrated Circuit Architecture

- Manufactured on TSMC's 180 nm process in 2mm * 2mm of silicon and designed to run at 23 K. TSMC's PDK only promises accurate modelling down to 218 K, but simulations between 300 K and 23 K suggest reliability at 23 K.
- The input attenuator reduces the power of a signal to allow qubit stimulation without changing its state
- The output LNA amplifies the reflected signal while rejecting noise
- The circulator routes the TX and RX paths into the qubit with minimal crosstalk
- A scan chain provides a low-frequency digital control interface for tuning gains and resonant frequencies of components





Team



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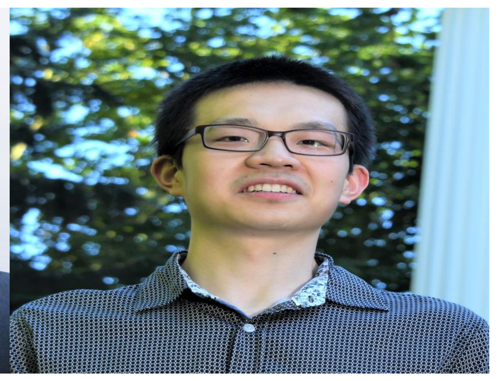
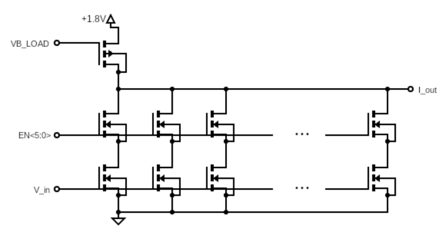
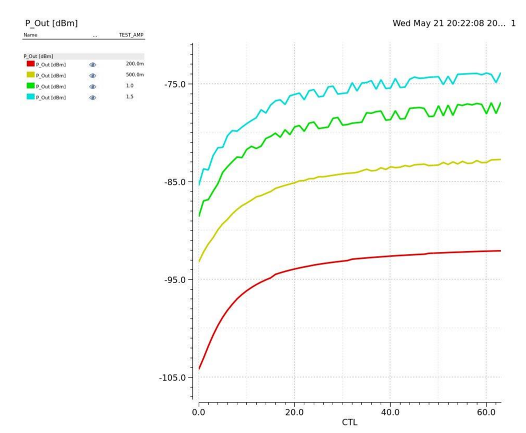


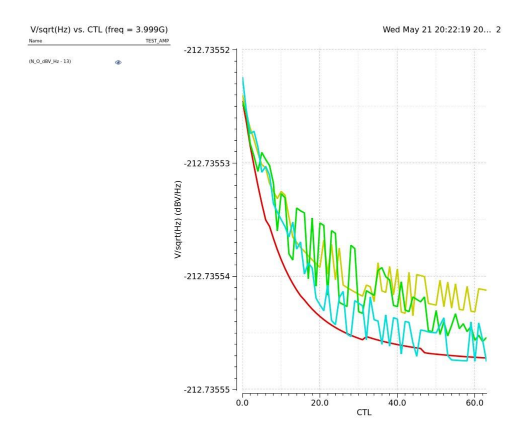
Xichen Li

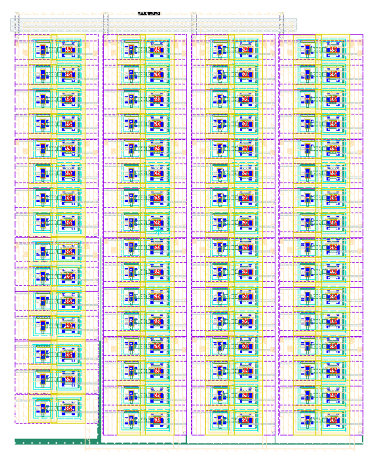
Attenuator Design (TX)

- Transmits off-chip signals into the circulator
- Reduces the power of the signal entering the circulator to within -60 to -90 dBm (left)
- Achieves a maximum output noise below -100 dBm (right)



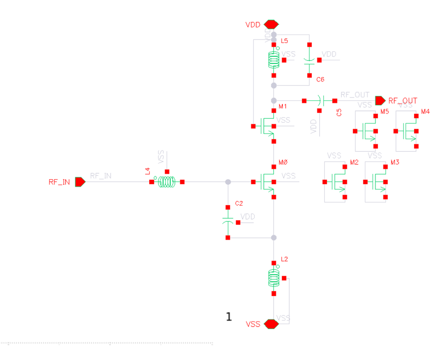


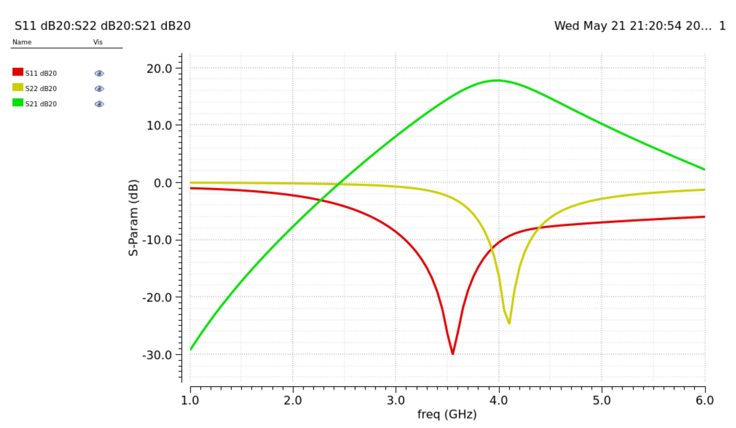


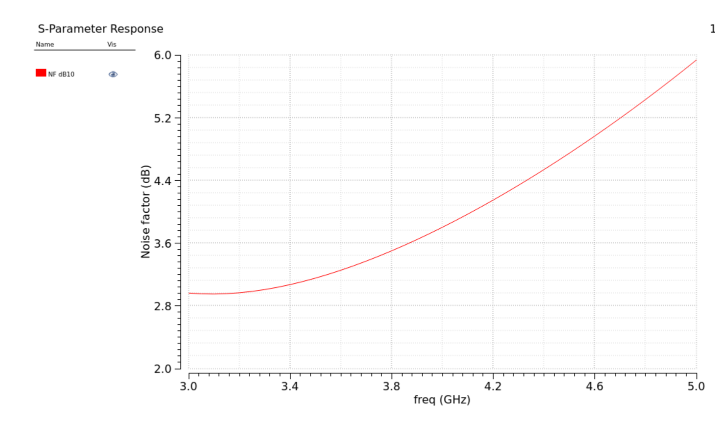


Low-Noise Amplifier Design (RX)

- Receives signals from the circulator and sends them off-chip
- Achieves a gain of 20 dB in the passband (bottom right) with a Noise Figure of 3 dB (bottom left)
- S11 and S22 (Reflection back into the input and output, respectively) are below -14 dB in the passband (bottom left)

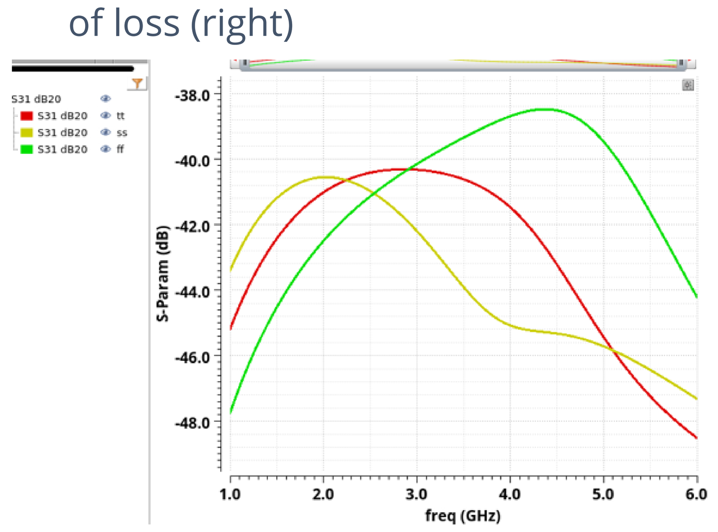


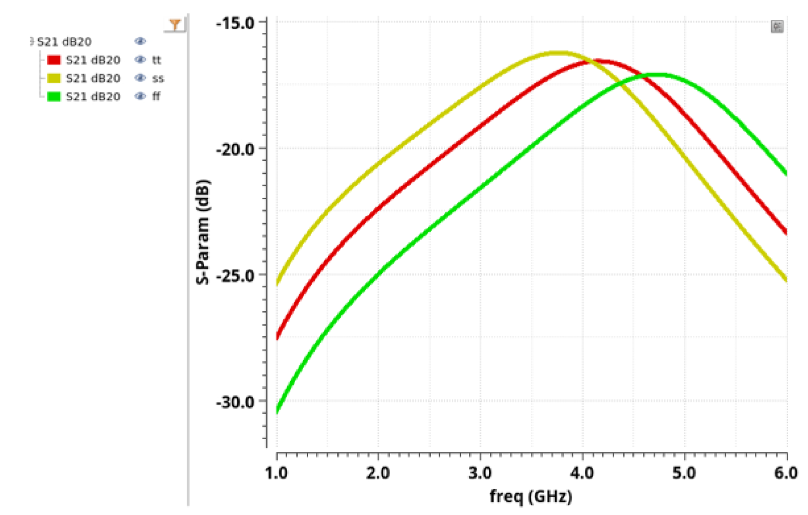




Circulator Design

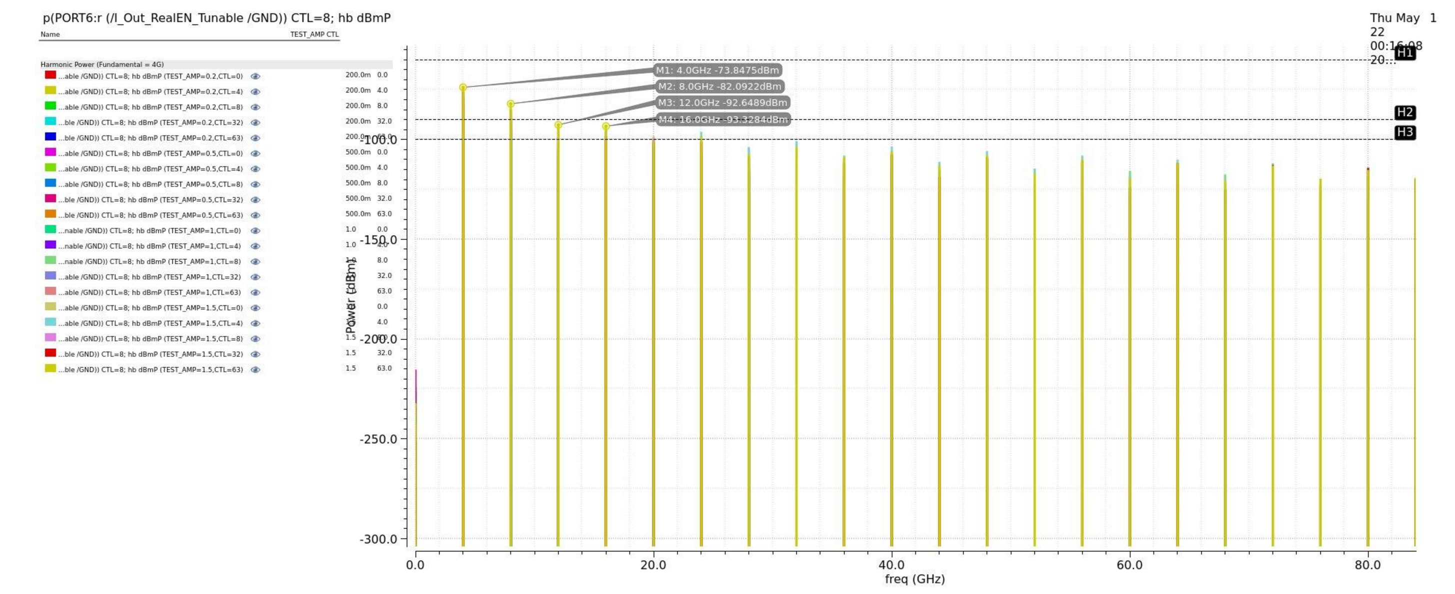
- Tunable passive component responsible for supplying input signals to the qubit and detecting the reflection using a single transmission line
- Consists of an on-chip transformer and capacitor bank to set the resonant frequency
- Achieves 40 dB of separation between the transmit and receive channels (left) with 16 dB of loss (right)



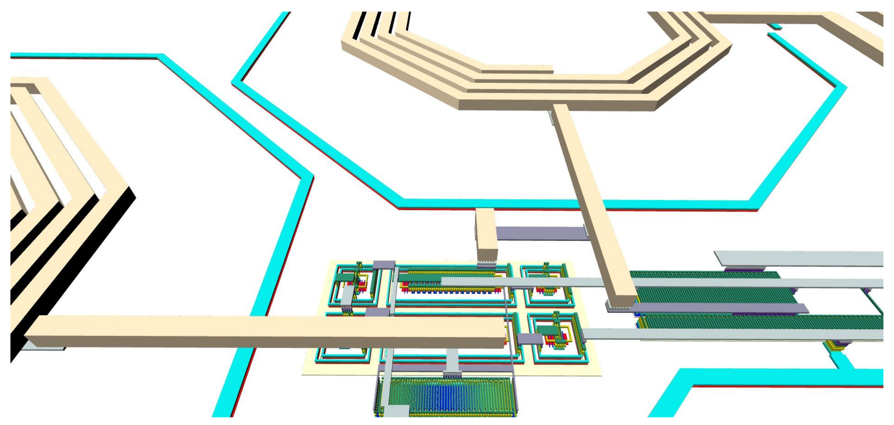


Preliminary Results and Test Plan

- Frequency = 4G, Bandwidth = 2G
- Power consumption = 17 mW
- Area utilization = 0.98 μm² of 2.72 μm² available



- Fully testing the device's intended functionality will require the use of a cryogenic chamber, which will cool the chip to an internal temperature of about 20 K. The qubit will operate at 4 K, but electrical activity in the chip will prevent it from reaching this temperature. Future work, which intends to integrate the qubit onto such a chip, will need to operate at 4 K.
- The chip includes internal GSG (Ground-Signal-Ground) and GSGSG pads for probing of the bare die (far left of bottom right image)



Future Work, References, and Acknowledgments

- Tapeout alongside UCLA and several other universities in June 2025
- Testing in a cryogenic chamber in September 2025

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