

Design and Validation of a 1MHz Double-pulse Test (DPT) Methodology for 900V SiC MOSFET

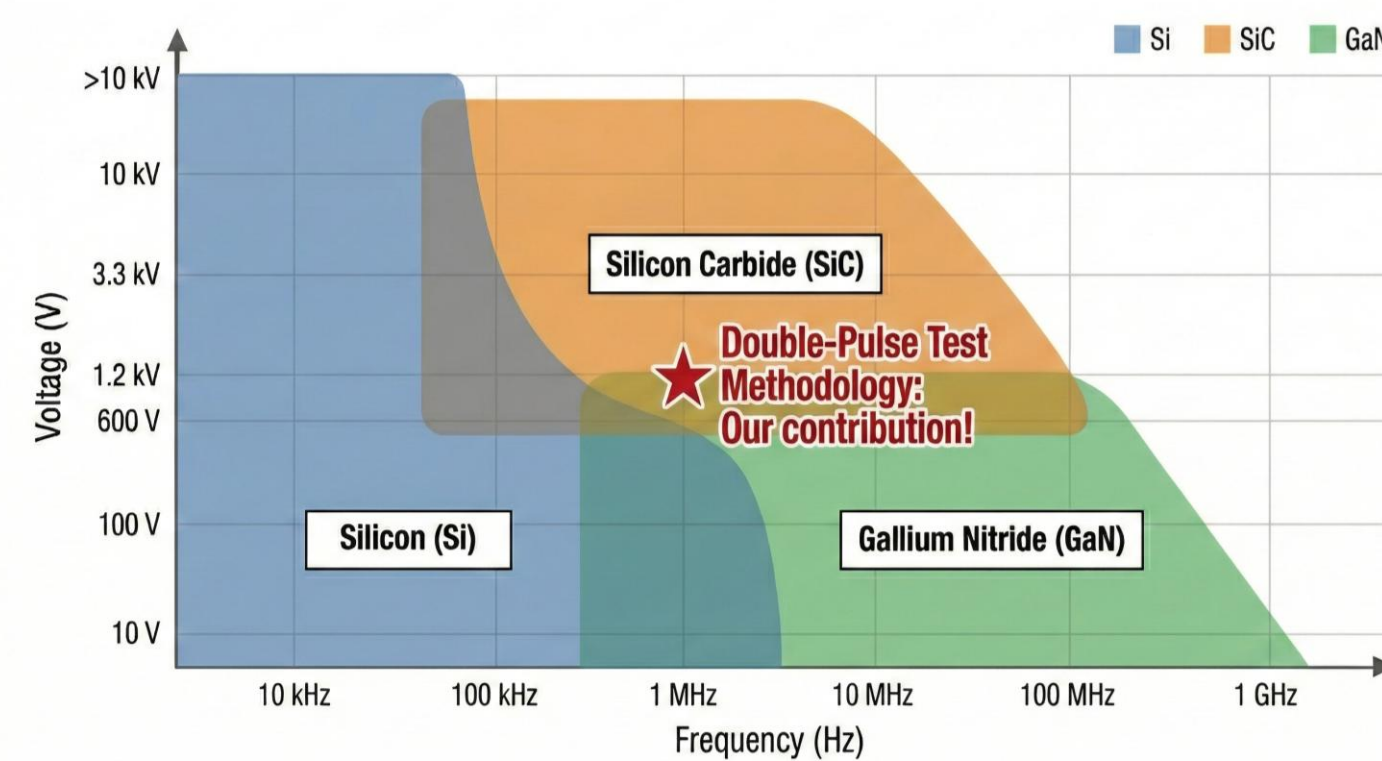


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MOTIVATION

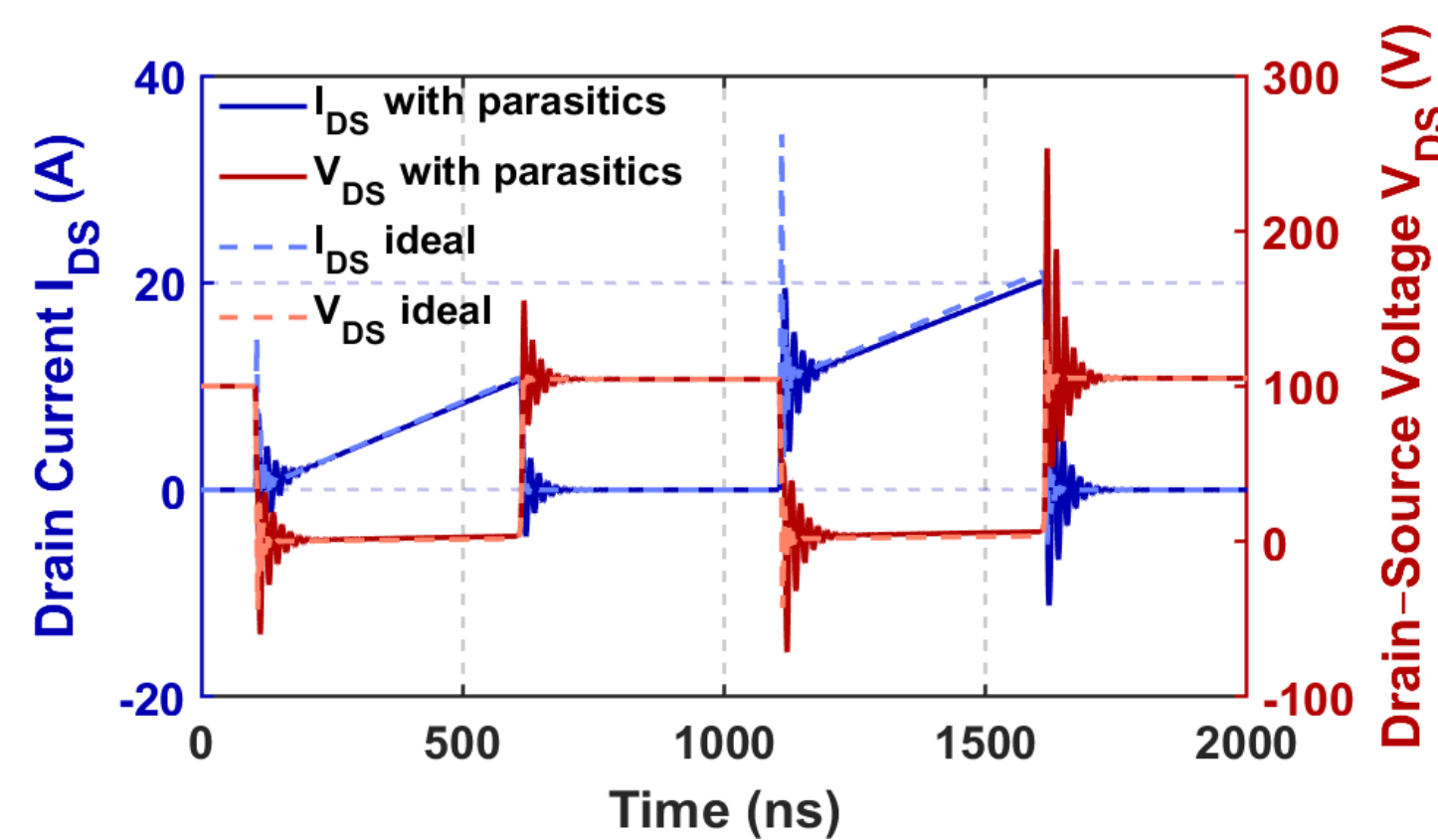
SiC MOSFET:

- faster switching; higher fs; lower switching loss
- high-voltage capability; thermal robustness

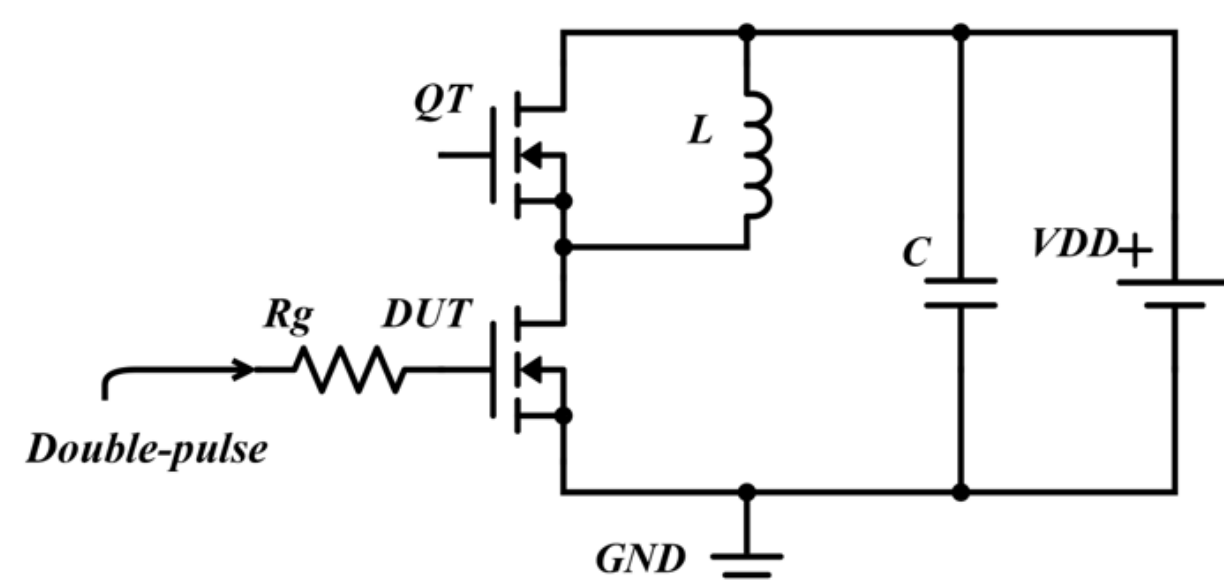


Challenge (MHz DPT):

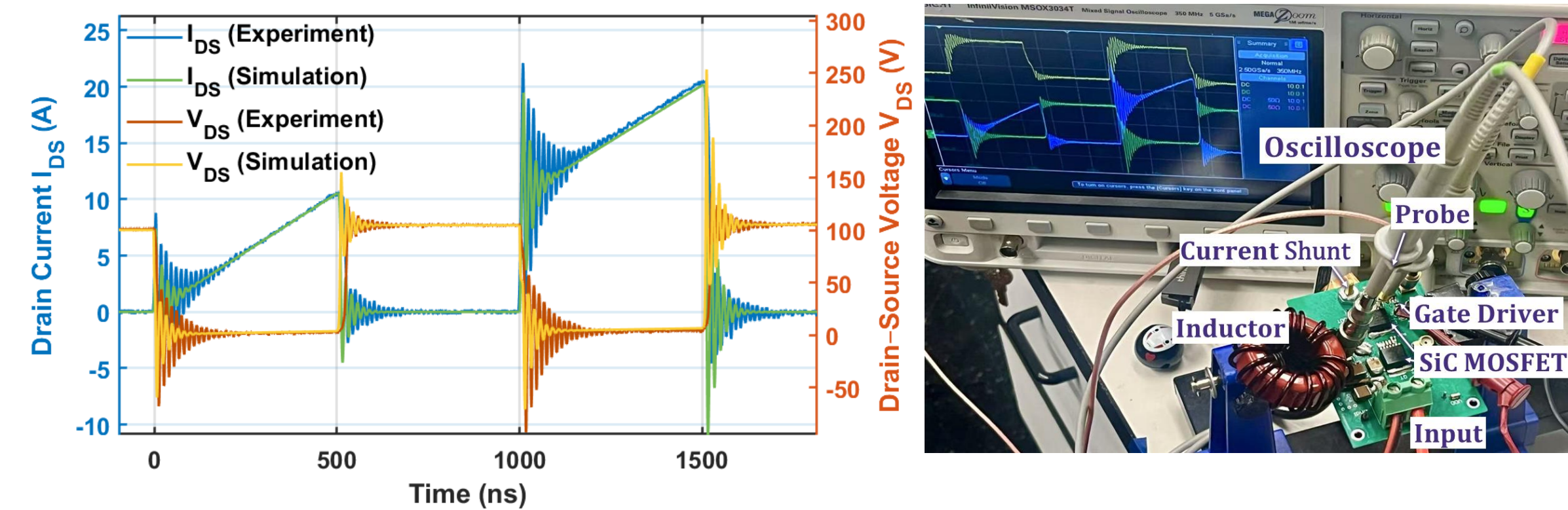
- Parasitics: PCB/package/measurement
- Waveform distortion: extraction error



Double-pulse Test



- ringing frequency match < 5% deviation



RINGING SUPPRESSION

- An R_{dmp} is added based on a time-domain ohmic-region RLC model to suppress ringing.
- RLC model with damping resistor:

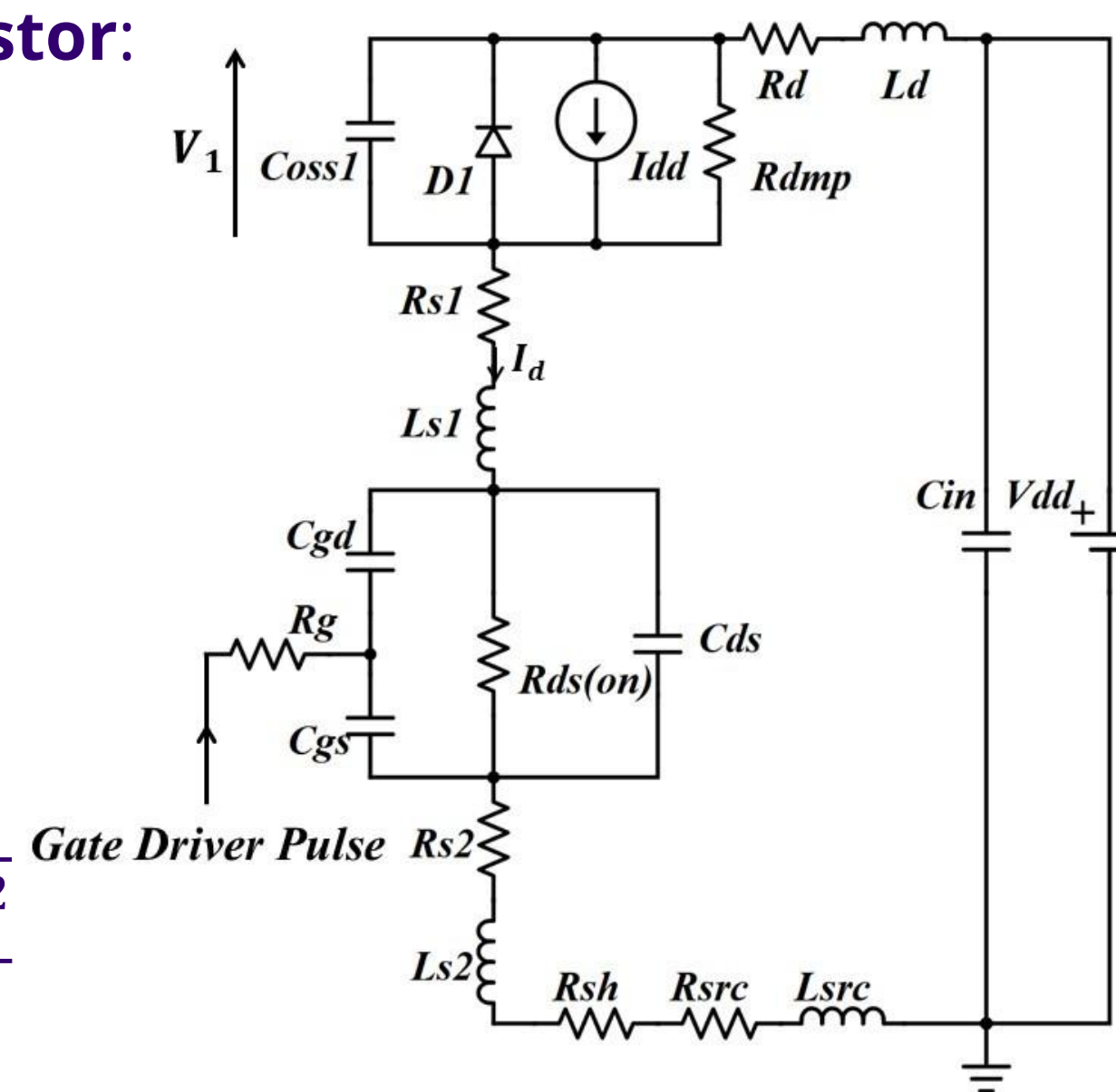
$$\frac{d^2 i_d}{dt^2} + \frac{R_\Sigma}{L_\Sigma} \frac{di_d}{dt} + \frac{1}{L_\Sigma C_{oss}} i_d = 0$$

$$\alpha' = \frac{1}{2} \left(\frac{R_\Sigma}{L_\Sigma} + \frac{1}{R_{dmp} C_{oss}} \right)$$

$$\omega_r' = \sqrt{\frac{1}{L_\Sigma C_{oss}} \left(1 + \frac{R_\Sigma}{R_{dmp}} \right) - \alpha'^2}$$

- Peak current (k-th oscillation):

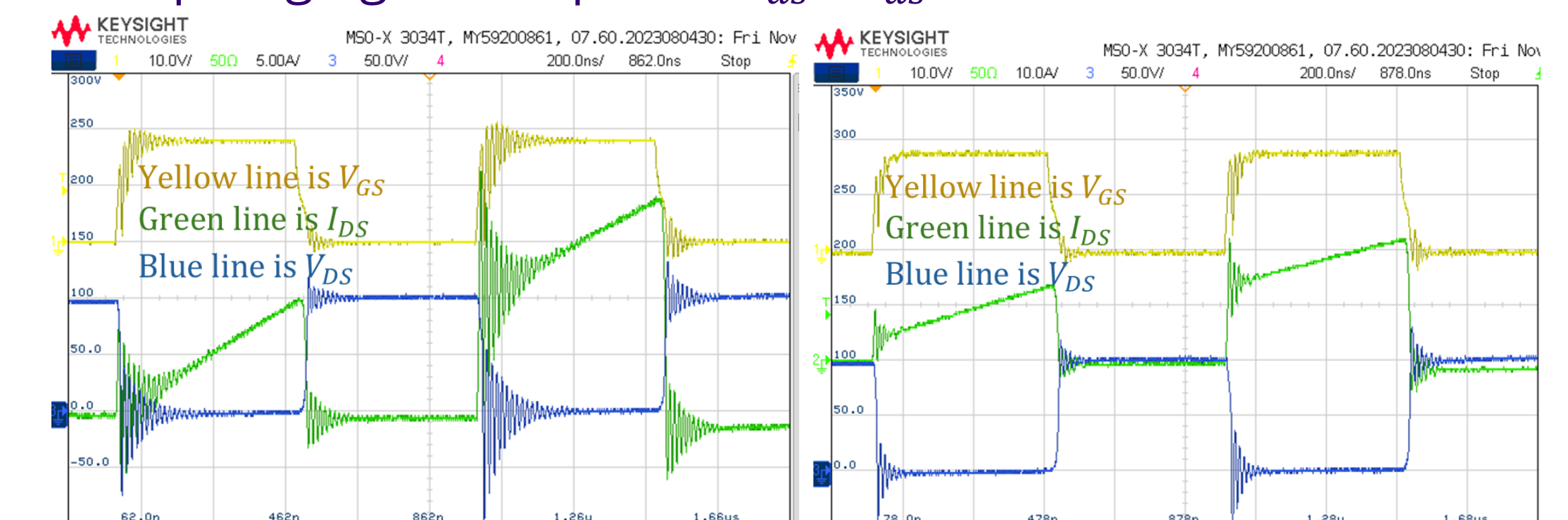
$$\Delta i_k' = \Delta i_1 e^{-\alpha'(t_k - t_1)} \frac{\omega_r' \sqrt{A^2 + B^2}}{\sqrt{\omega_r'^2 + \alpha'^2}}$$



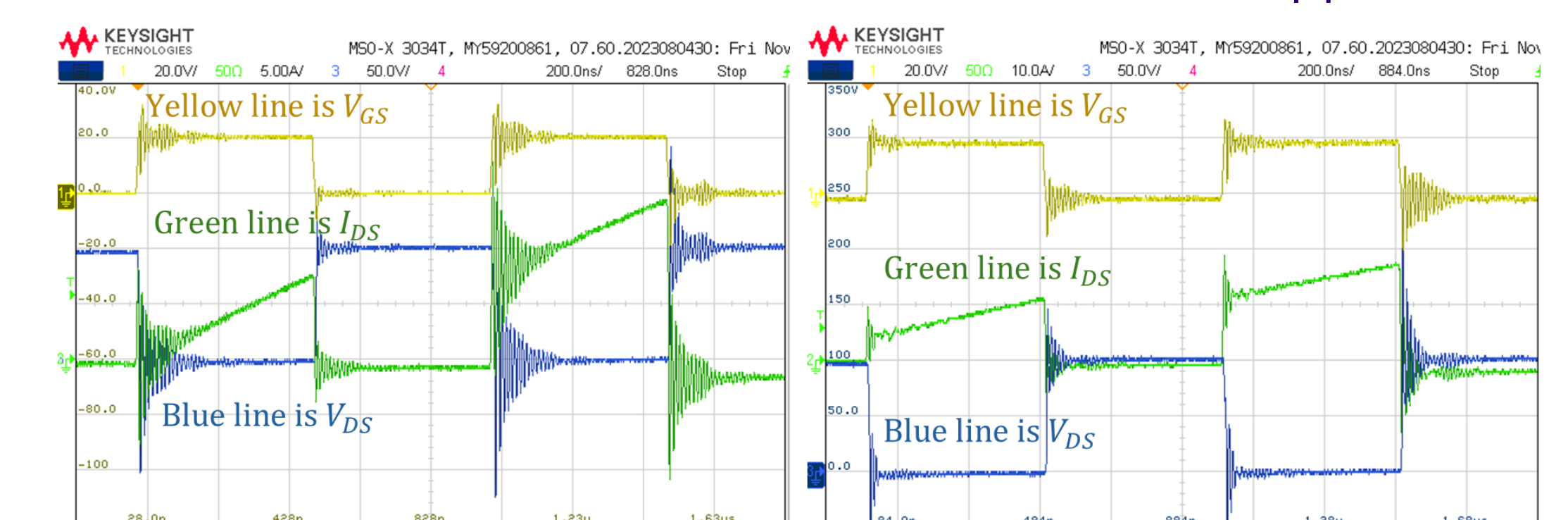
- **Trade-off:** Smaller R_{dmp} speeds ringing decay but increases turn-on bypass current and I_{ds} stress.

EXPERIMENTAL RESULTS

- **900 V C3M0065090J:** R_{dmp} suppresses 1 MHz commutation-loop ringing and improves I_{ds} / V_{ds} waveforms



- **1200 V AIMBG120R080M1:** validates the same approach



	C3M (w/o)	C3M (25Ω)	AIM(w/o)	AIM(25Ω)
t_f (ns)	10.0	9.2	3.2	2.4
E_{off} (μJ)	0.663	1.491	0.395	0.826
Overshoot (%)	101.0	63.7	125.0	81.4
t_r (ns)	10.8	10.8	7.6	7.6
E_{on} (μJ)	23.224	16.717	14.868	7.349
t_{rr} (ns)	8.46	6.98	6.30	5.64

CONCLUSION

Platform:

- 1 MHz DPT (900 V SiC) with low-parasitic layout

Modeling:

- VNA parasitics to LTspice

Design rule:

- time-domain ohmic-region guideline for R_{dmp}

Measured results ($R_{dmp} = 25 \Omega$):

- >60% peak reduction; 15 to 5 cycles (900 V C3M0065090J)

Cross-device validation:

- 16 to 3 cycles on 1200 V AIMBG120R080M1
- no hardware changes