Low-Noise Discontinuous Instrumentation Amplifier for Biomedical Signals using180nm Silicon Technology

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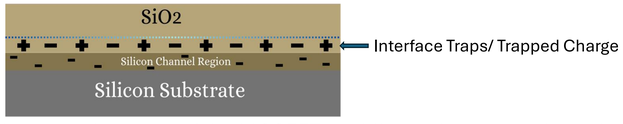
Motivation/Problem

- Biomedical signal acquisition systems (such as ECG, EEG, and EMG) must reliably extract microvolt-level differential signals in the presence of large common-mode interferers.
- At low frequencies, standard CMOS instrumentation amplifiers are heavily limited by flicker noise (1/f). This noise originates from the random trapping and releasing of charge carriers at the SiO_2 - Si crystal interface of the input transistors. Standard continuous-time techniques require excessively large transistor areas or complex chopping networks that introduce switching spikes and residual offsets.

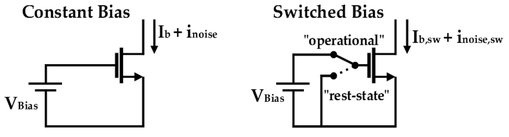
Proposed Solution

Switched-Bias Low-Noise Amplification

- Periodically switch the amplifier between an operating state and a rest state
- During rest state, the MOS devices enter deep accumulation/depletion region, resulting in a reduction of trapped charge at the SiO_2–Si interface and conserving power
- This suppressed 1/f flicker noise -> improves detection of low-frequency biological signals



During the operating state of the MOSFET, mobile carriers move through the channel region near the SiO_2 interface. Interface traps randomly capture and release these carriers, causing fluctuations in channel current that appear as 1/f flicker noise.



Operational state: Amplifier is on and sensing signal
Rest state: Amplifier is off/rest, enters depletion or accumulation region to reduce trapped charge effects
Result: Lower 1/f noise at low frequencies

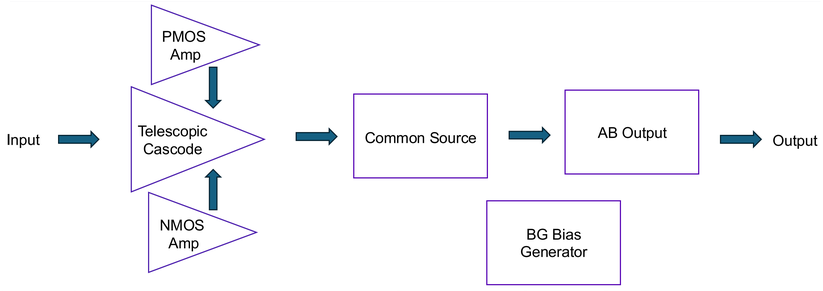
Design Specifications

Circuit Block Specifications:

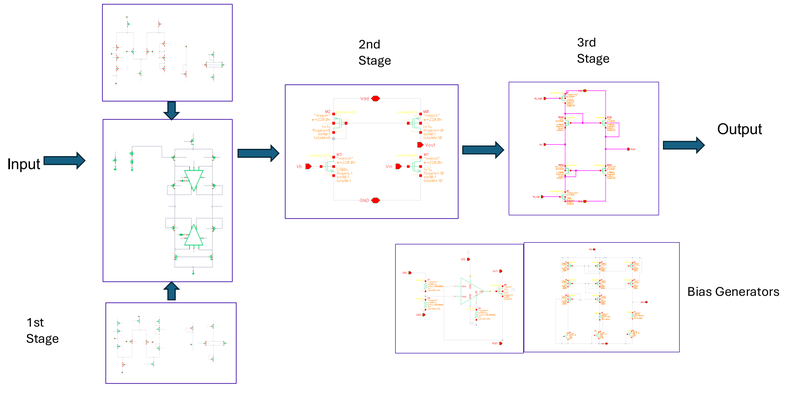
Telescopic Cascode AOL: 80dB IQ: 500uA Vin,in: <= 4nV/Hz^½	Common Source AOL: 20dB IQ<50uA FP1>5MHz
PMOS Gain Boost Amp AOL: 40dB IQ: 30uA FP1>5MHz	AB Output Stage IQ=50uA Rout<1kOhm
NMOS Gain Boost Amp AOL: 40dB IQ: 30uA FP1>5MHz	BG Bias Generator IQ<50uA Ton<30us

Goal: ECG level noise performance with lower power than standard commercial front-end designs. Design targets were based on commercial ECG front-end performance, aiming for sub-µVRMS input-referred noise while reducing power consumption through switched-bias low-noise operation.

System Architecture



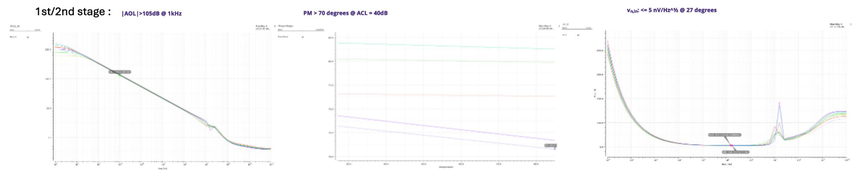
The Core Architecture: Our system implements a Discontinuous, Switched-Bias Two-Stage Amplifier architecture optimized for low frequency biomedical signals. The design is broken into three foundational pillars: an automated Bias Generator, a high-gain Input Buffer stage, and a low-impedance Output Driver stage.



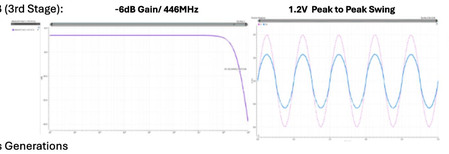
Circuit Block Architecture and Flicker Noise Reduction:
The full amplifier is divided into 1st, 2nd, and 3rd stage schematic blocks with bias generation. During rest mode, the stages are duty-cycled, driving MOS devices into accumulation or depletion to reduce trapped charge at the SiO_2/Si interface and lower 1/f flicker noise when sampling resumes.

Verification

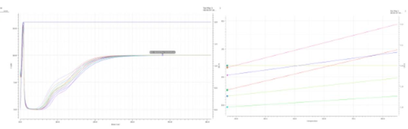
1st/2nd stage : |AOL|>105dB @ 1kHz PM > 70 degrees @ ACL = 40dB $v_{n,in}$ <= 5 nV/Hz^½ @ 27 degrees



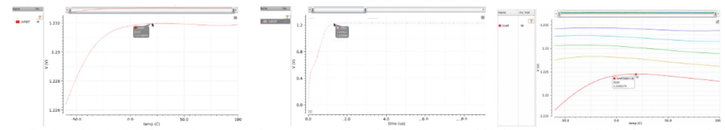
AB (3rd Stage): -6dB Gain/ 446MHz 1.2V Peak to Peak Swing



Current source bias generator: startup time of <40ns, corner variation of 0.14%



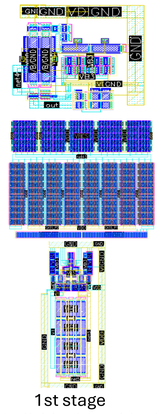
Bias Generations



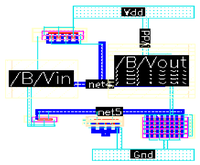
Bandgap Circuit: (left) Temp independence @ room temp voltage of 1.23 and current of 34uA consumption. (Middle) Start up time of 1.2us. (Right) Corners and its variation is 0.9% at room temp across all corners

Layout/Test Plan

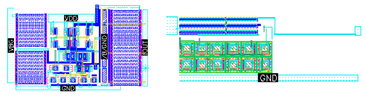
Block Layouts:



1st stage

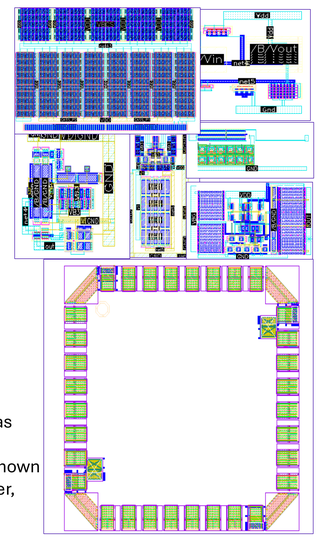


3rd stage



Bias Generators

Test Plan:



Individual test blocks, including the first stage, second stage, and bias generation circuits, were laid out separately to support block-level verification. These layouts will be integrated into the full pad frame shown on the right, allowing external access to key bias, input, output, power, and ground nodes for post-layout testing and measurement of the complete instrumentation amplifier system.

Acknowledgements

We would like to thank Professor Rudell, Frank O., Elpida Karapepera, and Ahmed R. Aboulsaad for their invaluable guidance, mentorship, and feedback throughout this project. We also thank Apple and TSMC for their support and sponsorship of this project. This work drew on concepts from *Switched-Biasing Techniques for CMOS Voltage-Controlled Oscillators.*

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