



EVALUATION OF HIGH-FREQUENCY SUBSTRATES FOR ANTENNA DESIGNS



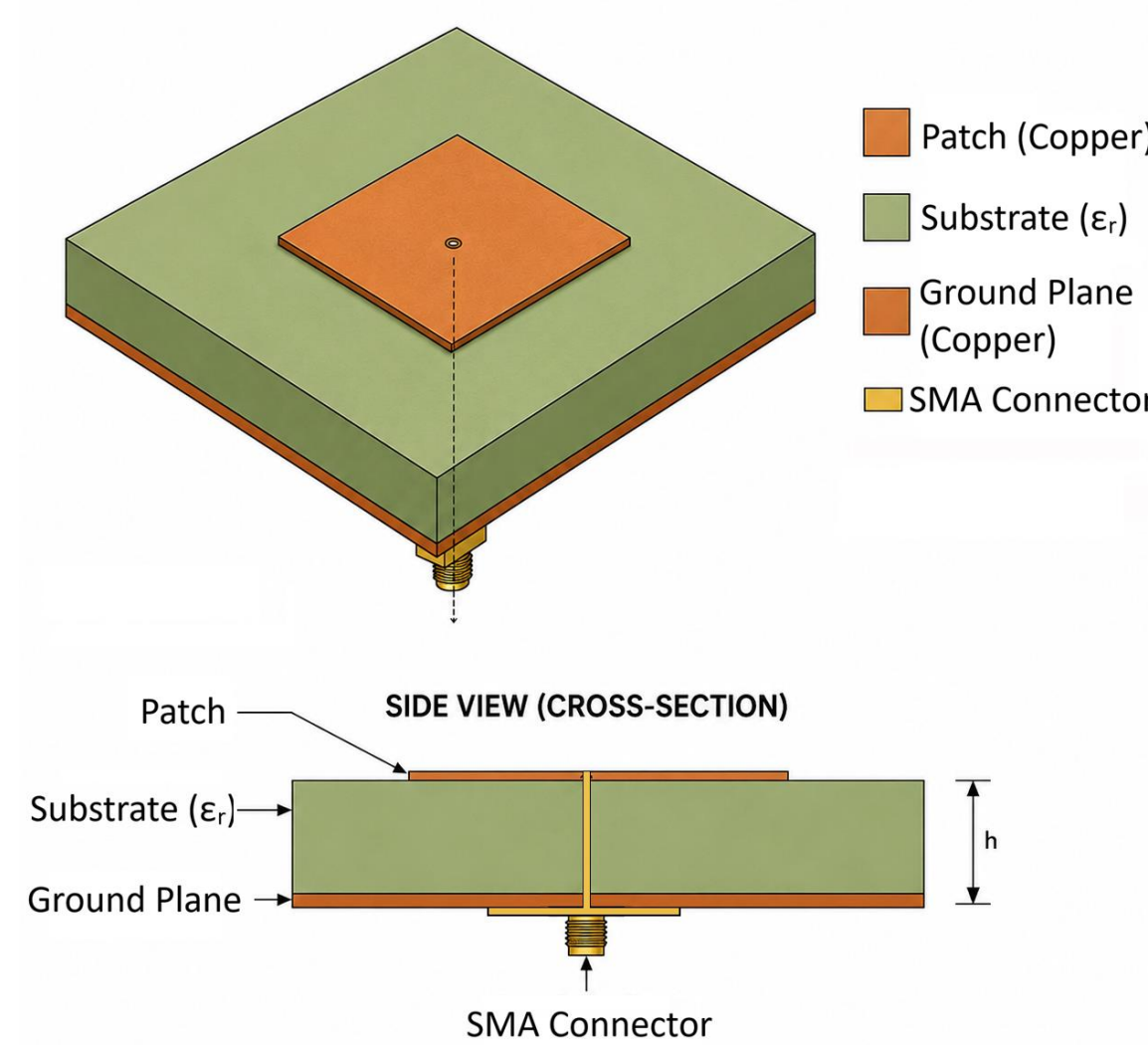
STUDENTS: CARSON LARGE, OWEN WILHERE, KAI FELLER, JOSEPH TSENG, JAMES DEMASS

Introduction

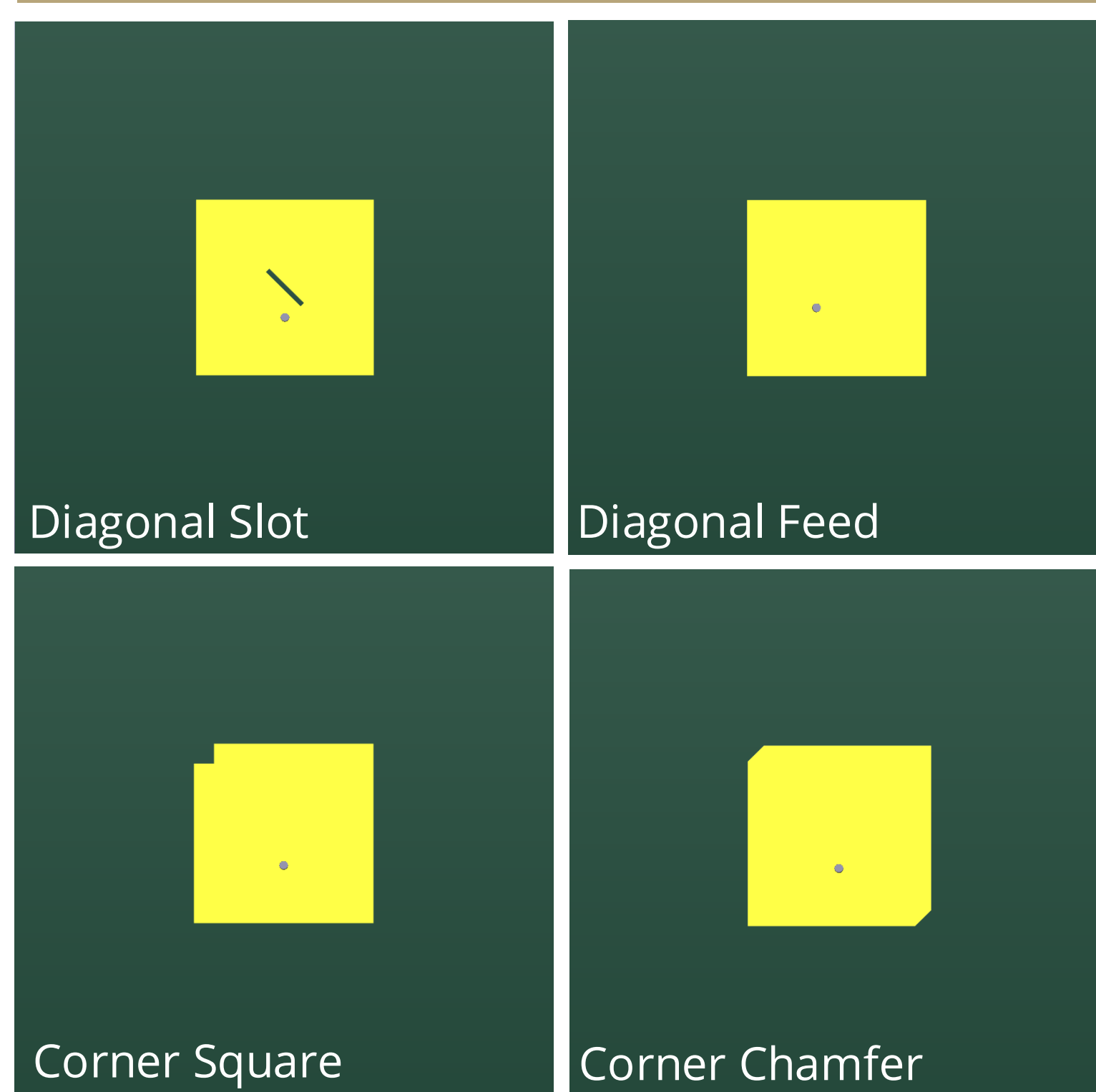
Wireless systems require antennas that balance performance, manufacturability, and cost. RF substrate selection strongly affects bandwidth, gain, efficiency, and circular polarization performance.

Blue Origin is interested in how commercially available RF substrates impact 2.45 GHz patch antennas. 20 circularly polarized patch antennas were designed and evaluated. The designs span 5 RF substrates and 4 perturbation geometries.

How do commercially available RF substrates compare across patch antenna performance, manufacturability, and cost tradeoffs?



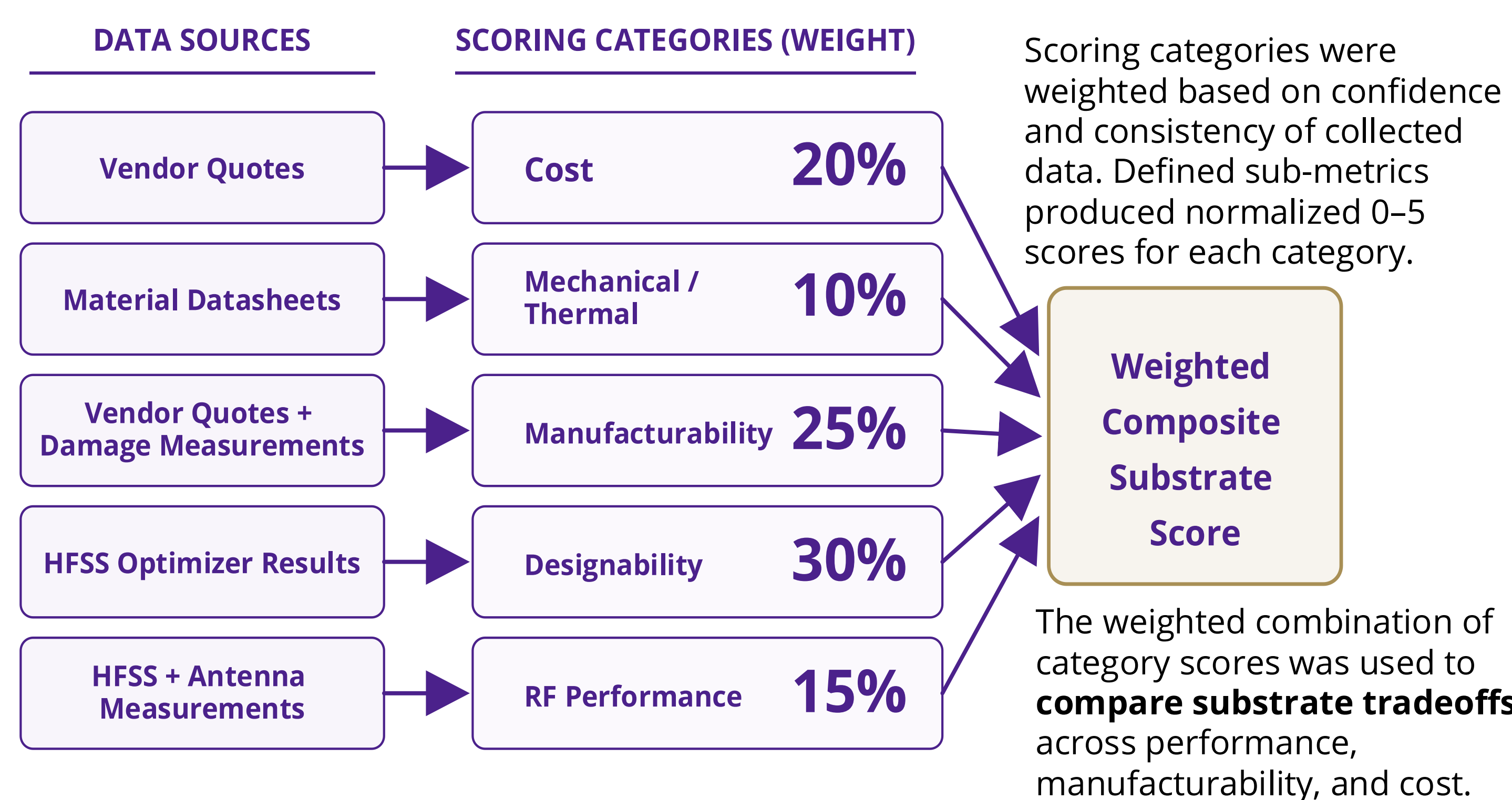
Patch Topologies & Design Requirements



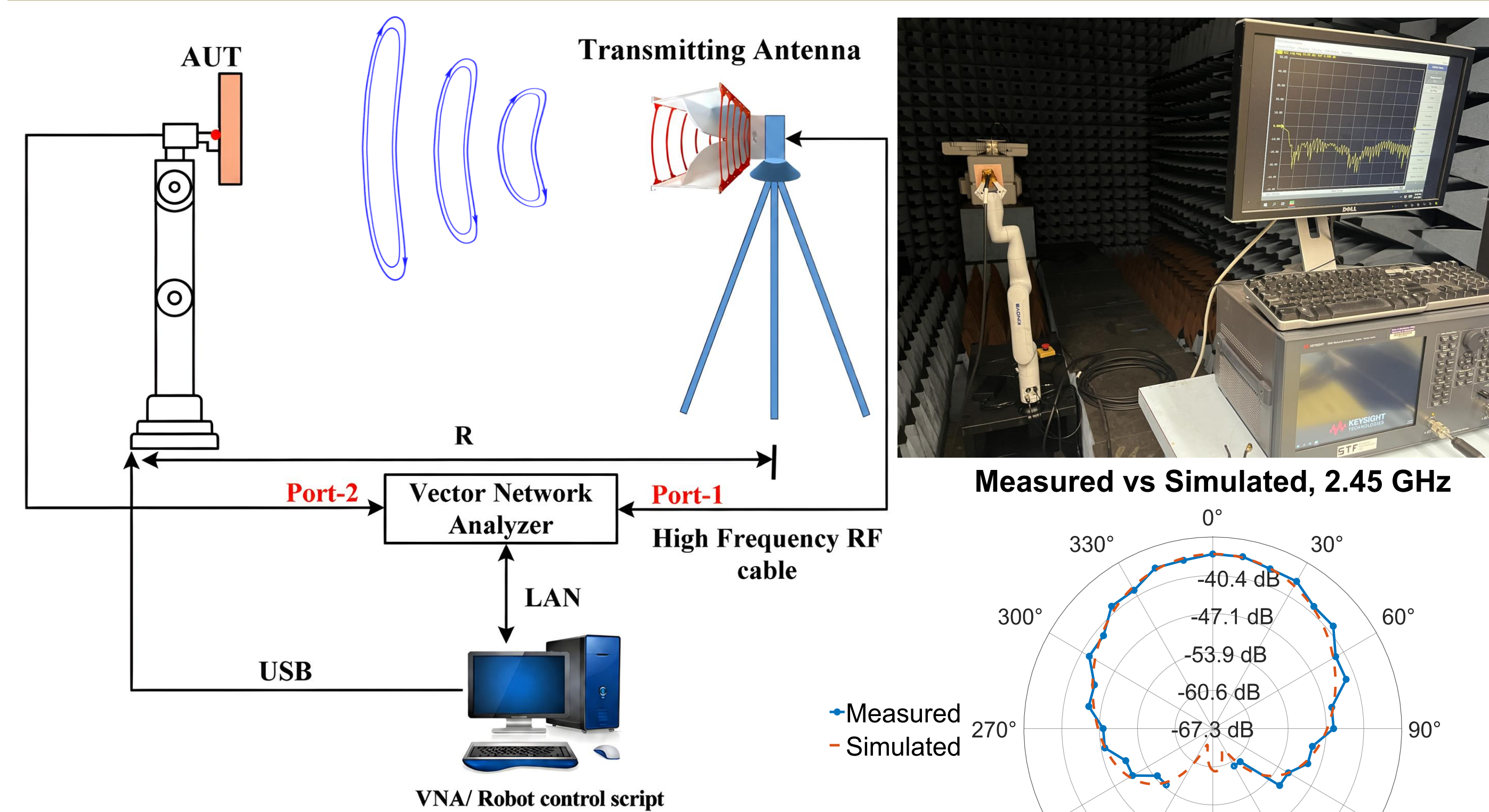
ANTENNA PERFORMANCE SPECIFICATIONS	
METRIC	REQUIREMENT
Frequency Band	2.42 – 2.48 GHz
Polarization	Left-Hand Circular
Axial Ratio	< 3 dB at boresight
Boresight Gain	≥ 4 dBi
Coverage	LHCP gain > -12 dBi over hemisphere
Size	≤ 6 in × 6 in
Feed	SMA probe feed

Four circularly polarized patch antenna geometries were evaluated using identical design requirements.

Substrate Scoring Framework

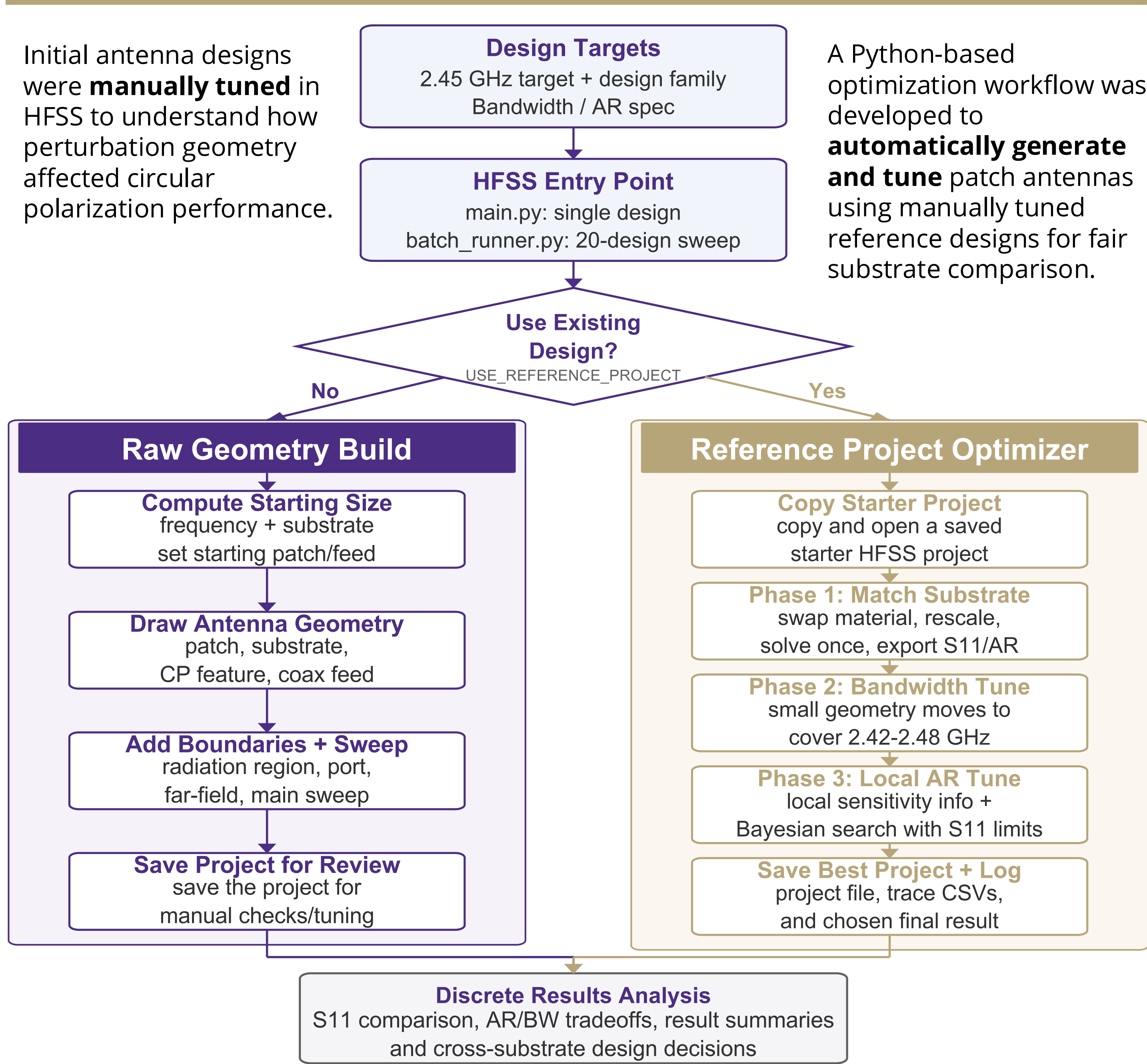


Measurement Setup

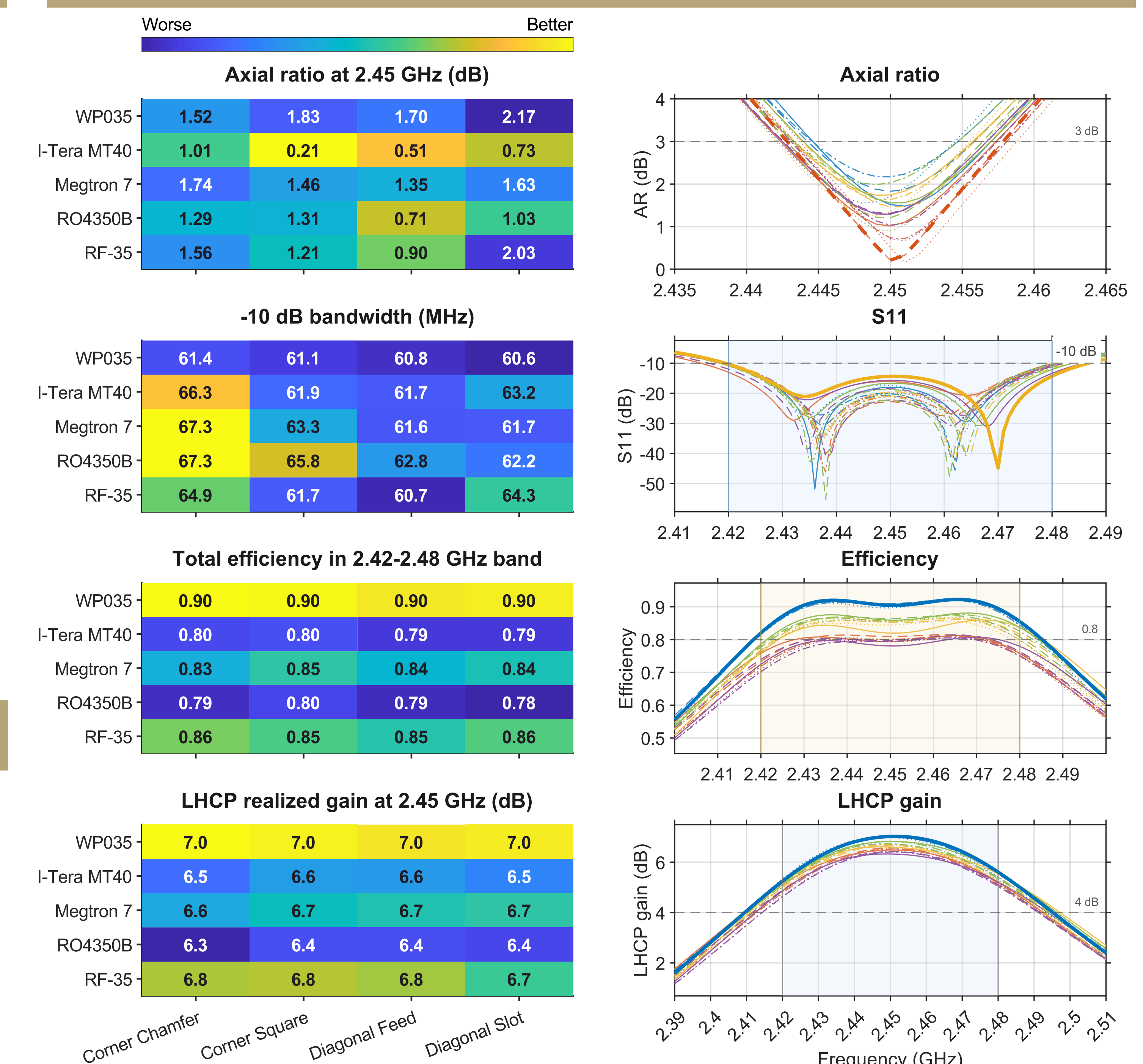


A Kinova robotic arm and Keysight VNA were used to collect antenna measurements including radiation patterns, S11, axial ratio, and gain performance.

HFSS Design Workflow



Optimizer Simulation Results



Substrate Score Results

Material	Manufacturer	Designability	Manufacturability	Cost	RF Performance	Mech / Thermal	Final Weighted Score
RO4350B	Rogers	4.0	5.0	5.0	4.5	3.9	4.5
I-Tera MT40	Isola	4.3	4.1	2.6	4.5	3.8	3.9
RF-35	Taconic	4.0	3.4	2.9	1.8	2.9	3.2
Megtron 7	Panasonic	3.9	2.0	2.5	3.1	3.6	3.0
WP035	Garlock	3.9	1.8	1.9	0.0	3.4	2.4

Future Research

The scripts that were developed are reusable across a wide range of RF substrates and antenna design parameters but can be expanded to encompass other parameters such as frequency and substrate thickness. Future work using industry-standard PCB manufacturing processes instead of LPKF milling could provide more consistent and applicable results. Adding more antenna features, such as superstrate layers on top of patch material, may introduce more interesting engineering challenges.



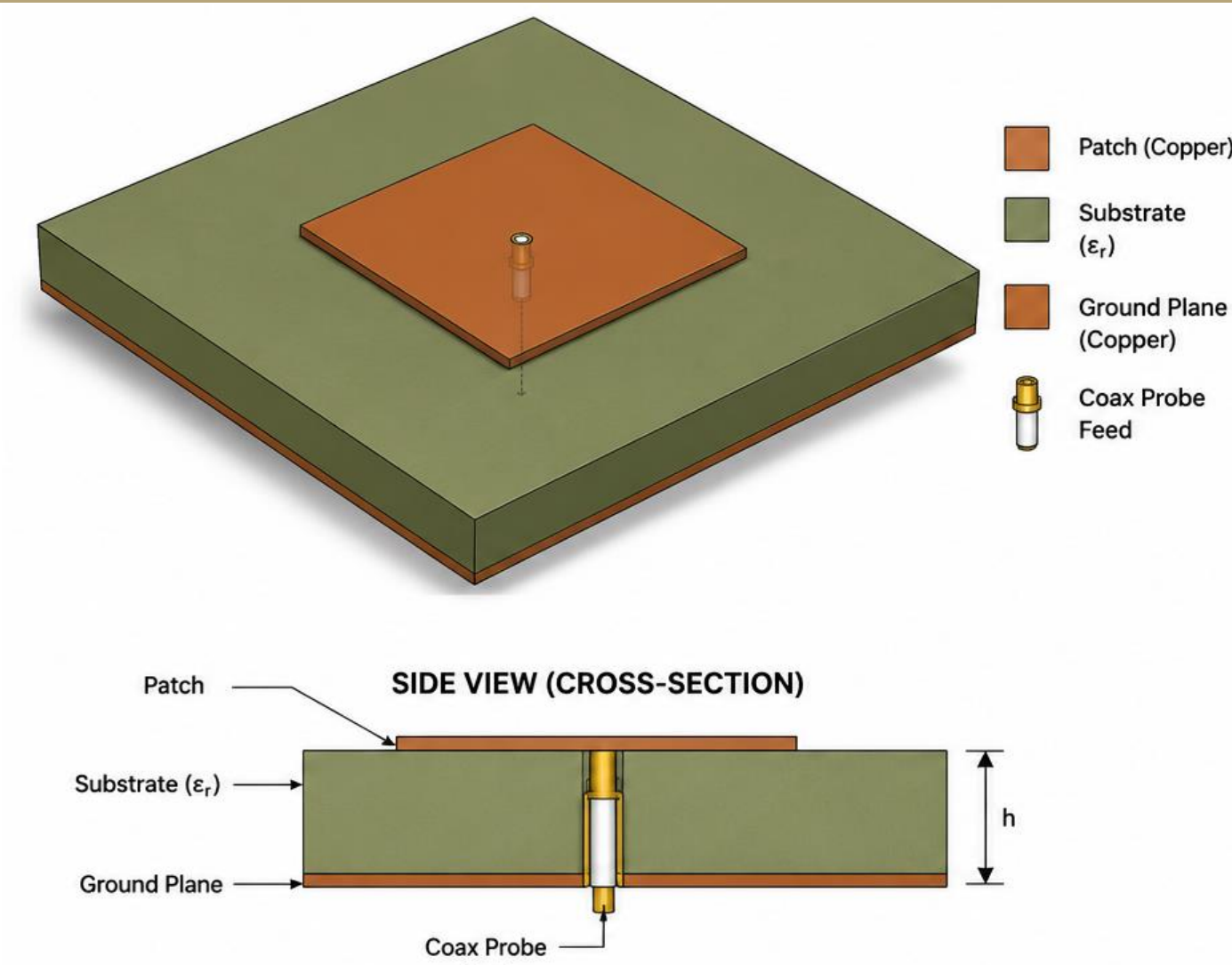
EVALUATION OF HIGH-FREQUENCY SUBSTRATES FOR ANTENNA DESIGNS

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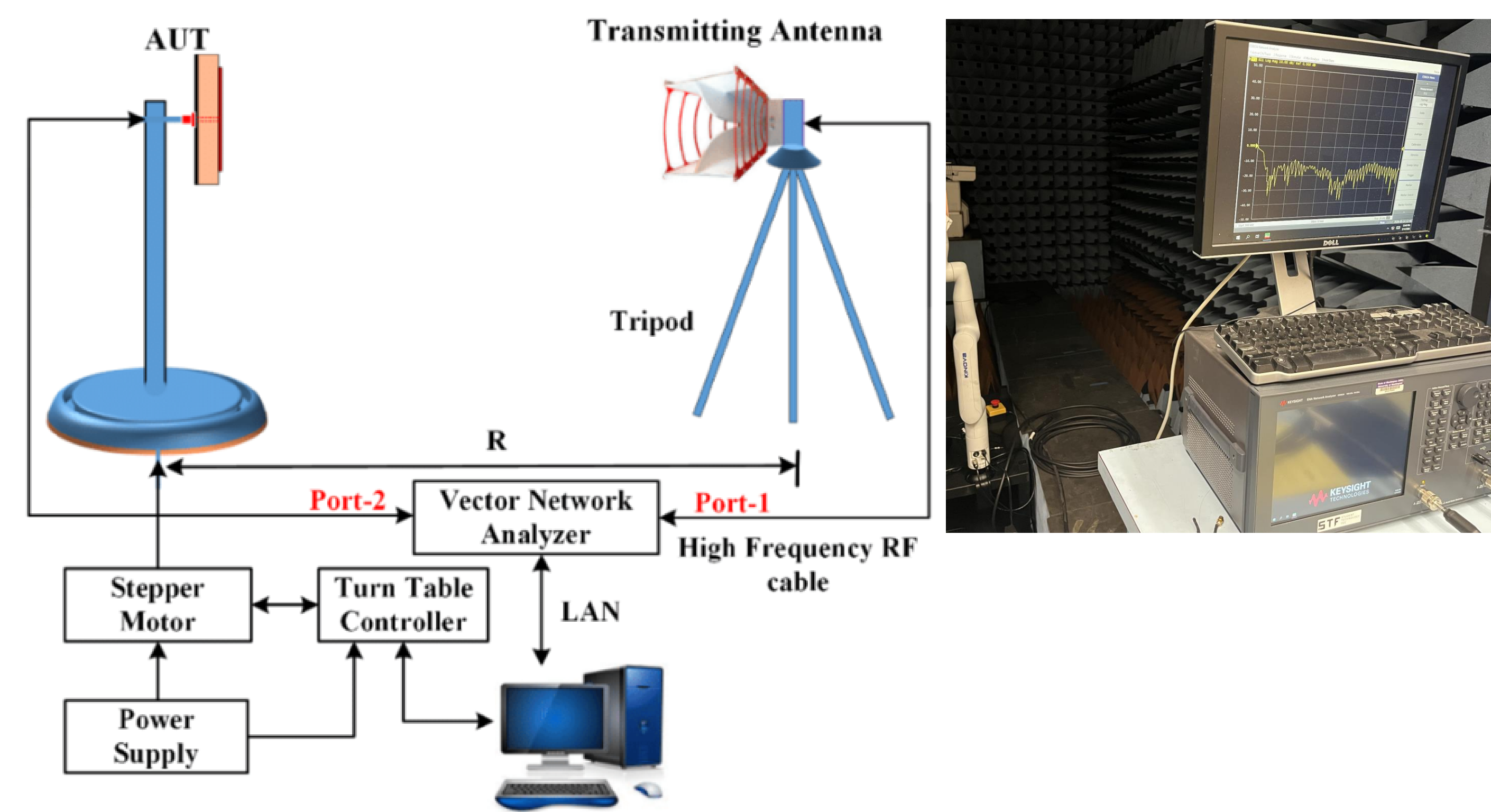


Introduction

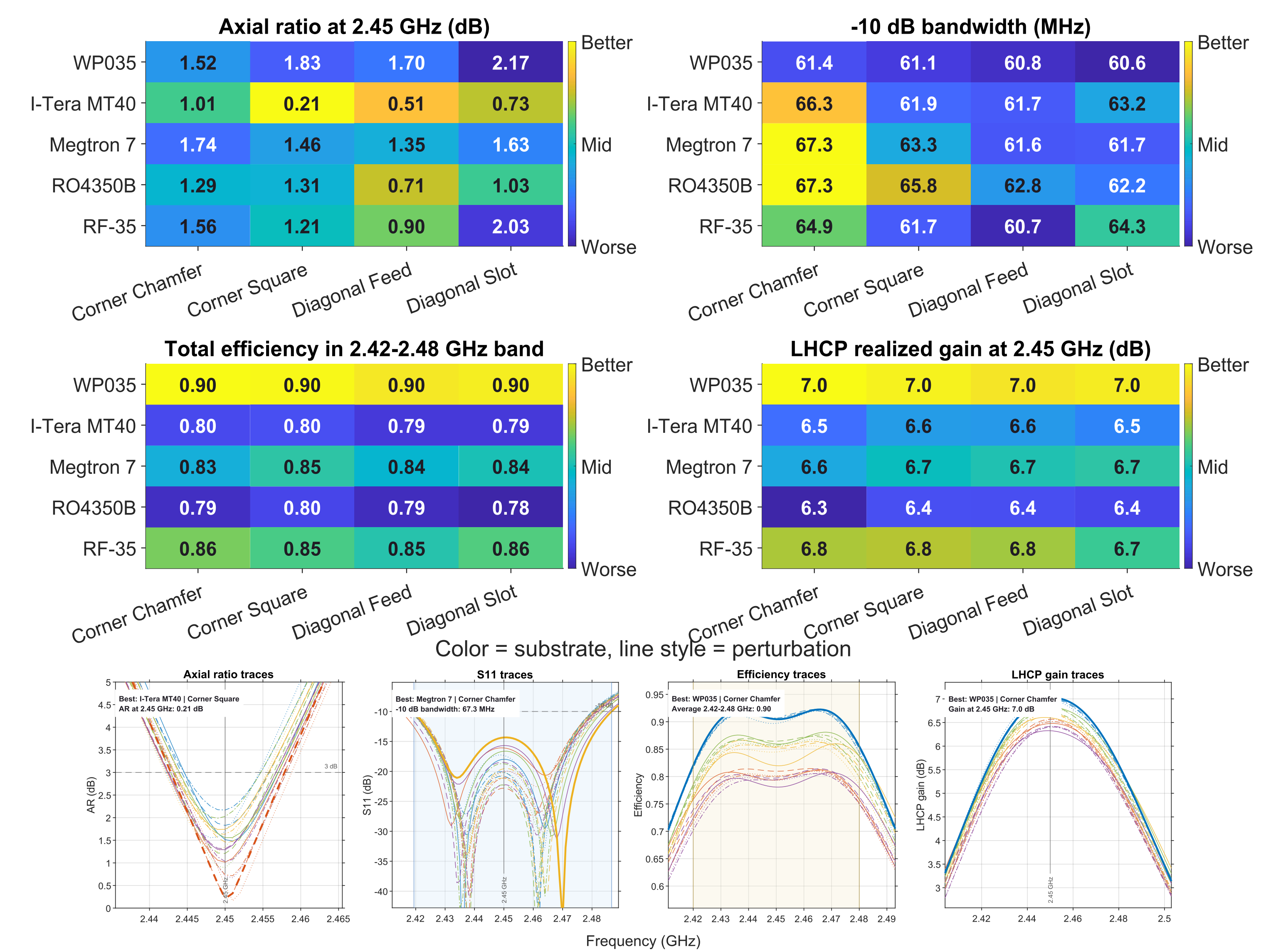
Blue Origin is interested in the performance of multiple substrate materials on WLAN patch antennas. Multiple 2.45 GHz patch antennas were designed and evaluated to compare gain, axial ratio, bandwidth, and substrate tradeoffs. Which commercially available RF substrates provide the best balance between antenna performance and practical implementation? RF substrate selection strongly affects antenna bandwidth, efficiency, manufacturability, and overall system cost.



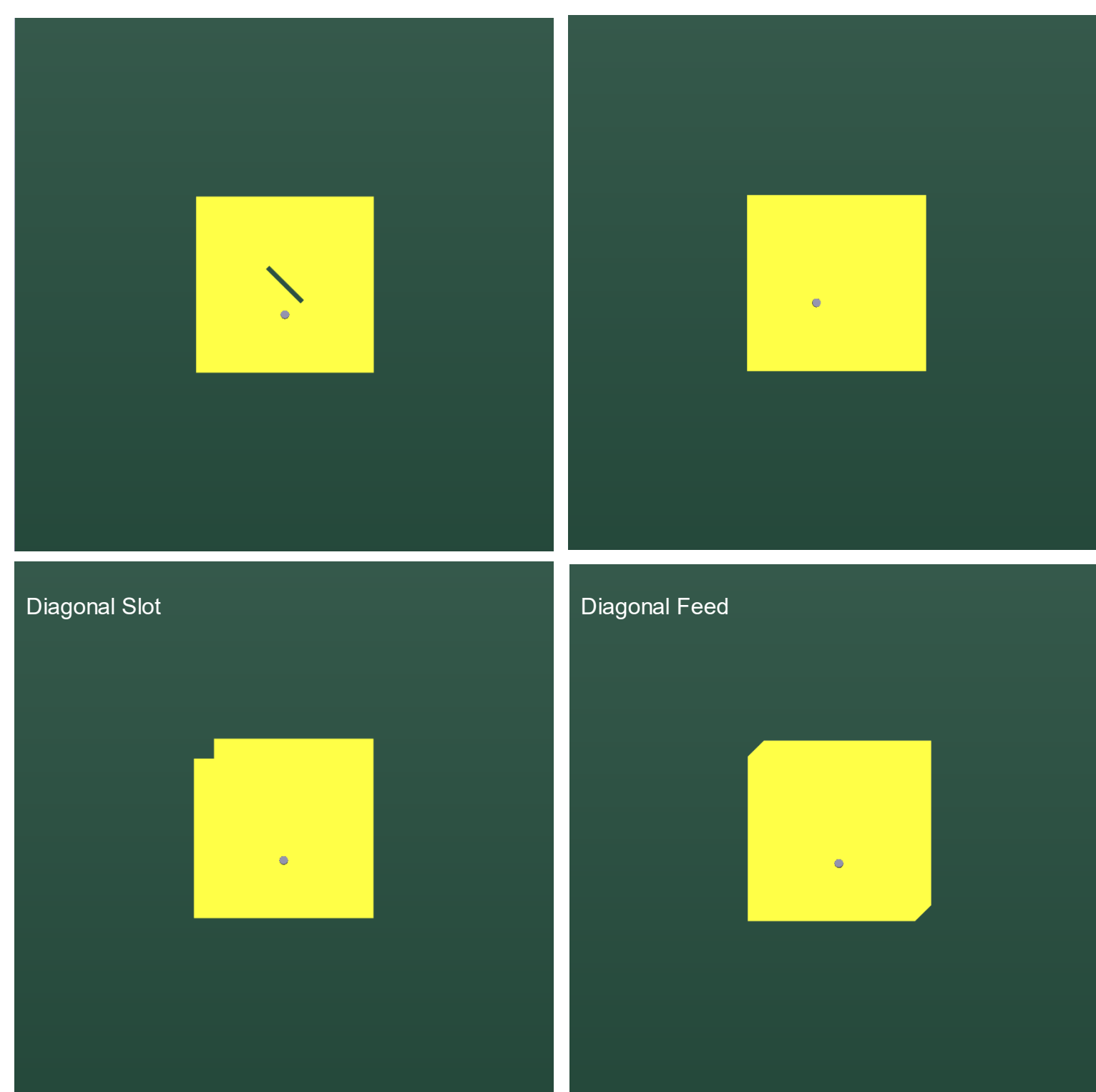
Measurement Setup



Optimizer Simulation Results



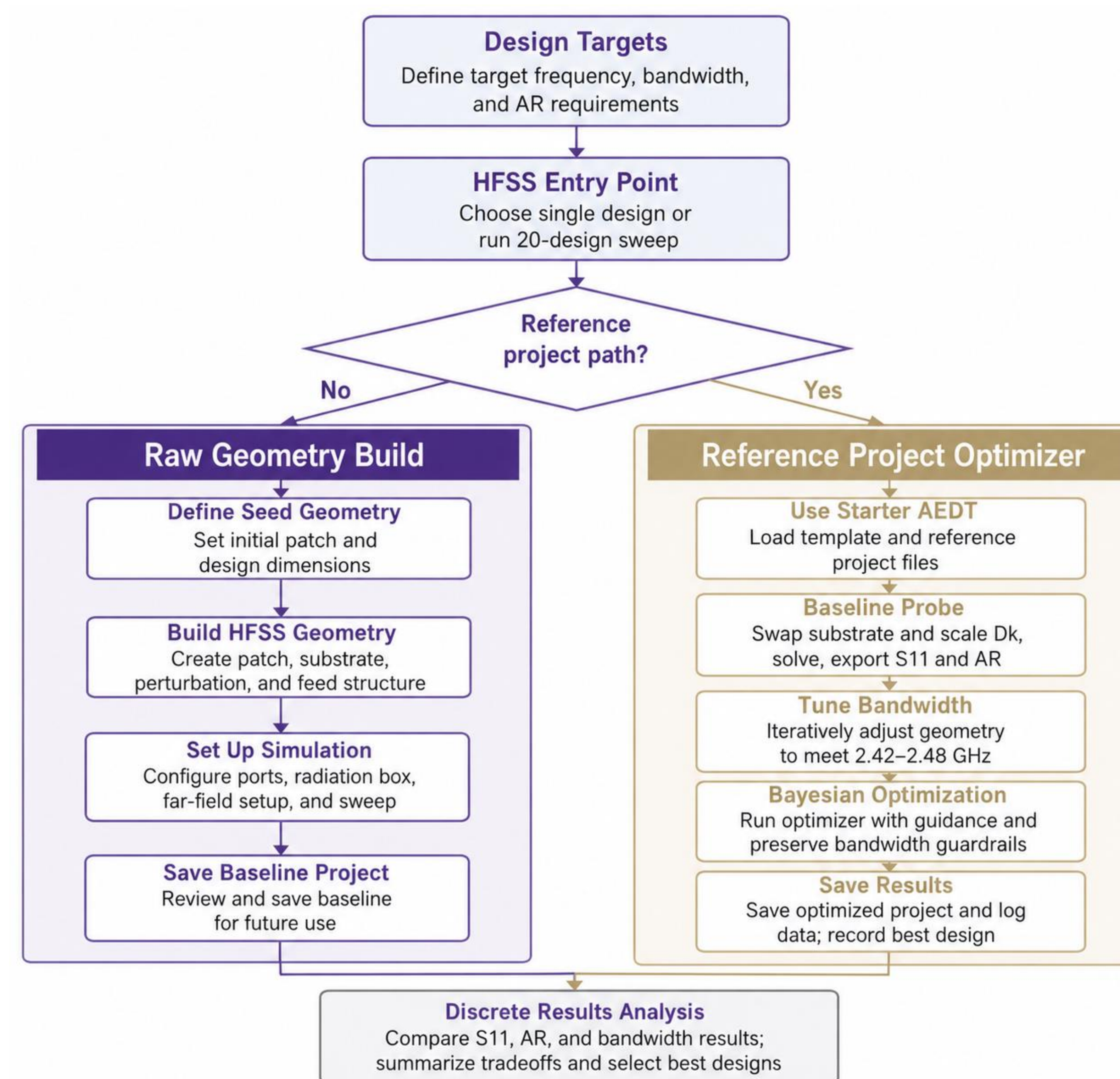
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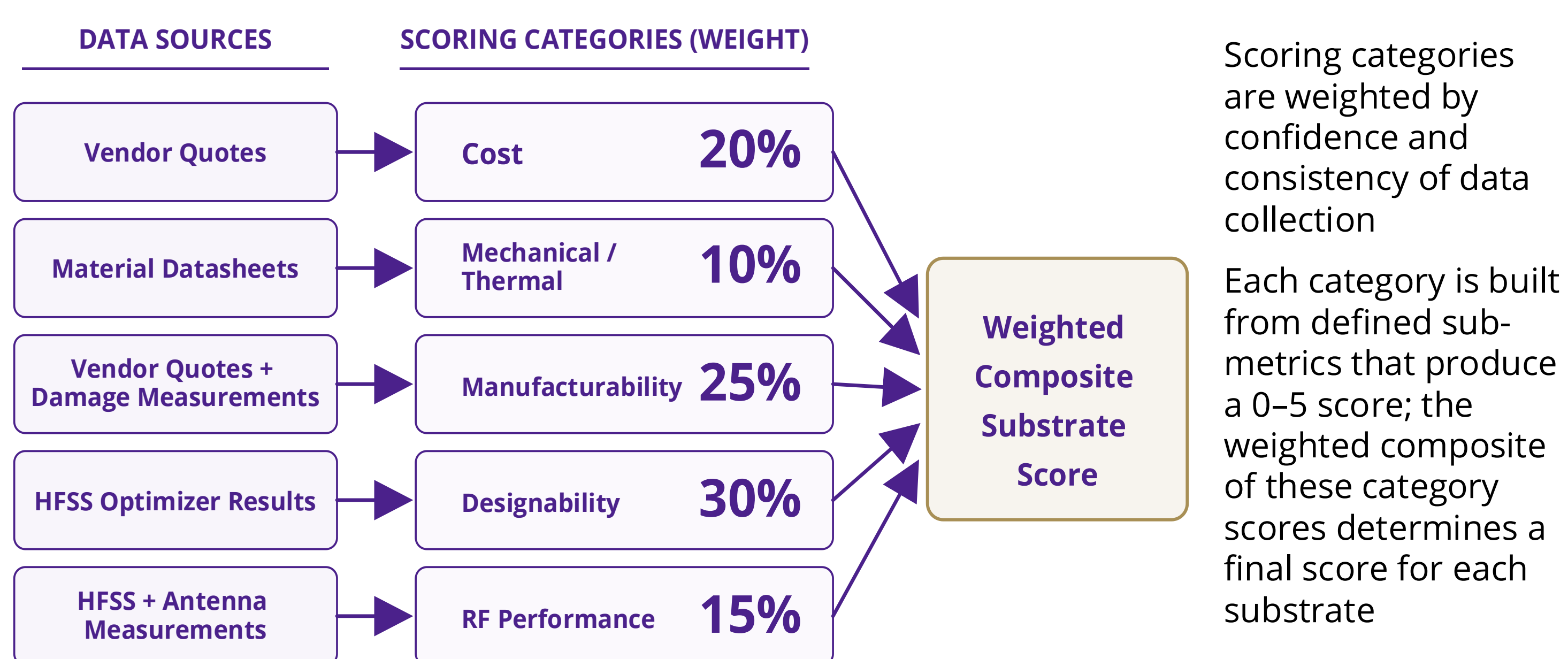
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METRIC	REQUIREMENT
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AR	< 3 dB at boresight
Boresight Gain	≥ 4 dBic
Coverage	LHCP gain > -12 dBi over hemisphere
Size	≤ 6 in × 6 in
Feed	SMA probe feed

Four different copper patch perturbation geometries are evaluated for performance

HFSS Design Workflow



Substrate Scoring Framework



Substrate Score Results

Material	Manufacturer	Designability /5	Manufacturability /5	Cost /5	Measured Performance /5	Mech / Thermal /5	Final Weighted /5
RO4350B	Rogers	4.00	4.93	4.95	4.48	3.74	4.47
I-Tera MT40	Isola	4.24	4.03	3.25	4.66	3.14	3.94
RF-35	Taconic	4.08	3.19	3.50	3.67	2.04	3.48
Megtron 7 E-glass	Panasonic	3.91	2.78	3.13	#VALUE!	3.02	2.80
WP035	Garlock	4.04	1.60	1.90	0.00	3.03	2.30

Future Research

Our scripts are compatible and reusable for most substrate materials and different design parameters. For any future research, using industry standard manufacturing processes instead of LPKF milling that was used for our boards, would provide more consistent and applicable results.



INSTRUCTIONS FOR CREATING A LANDSCAPE FOR THE 2025 ENGINE CAPSTONE SHOWCASE

QUESTIONS?: email pr_team@ece.uw.edu

1. DOWNLOAD (.PPTX) AND VIEW THE EXAMPLE AND BLANK SLIDE TEMPLATES

Open in PowerPoint and navigate them using the slide thumbnails on the left.

2. WE'VE COPIED THE BLANK TEMPLATES TO NEW SLIDES (3) FOR YOU TO BEGIN CREATING THE POSTER OF YOUR CHOICE.

If you'd like to create different versions of your poster, right click and choose "DUPLICATE SLIDE" in PowerPoint.

3. TO DISPLAY GUIDES: Select VIEW - GUIDES in the PowerPoint top menu bar.

4. WHEN FINISHED, SAVE AS BOTH .PPTX and PDF files

5. IMPORTANT!! DO NOT CHOOSE TO 'OPEN WITH GOOGLE SLIDES'

Your poster template will not be formatted properly. Download this file first and open/work within PowerPoint.

*PREFERRED FONTS ARE USED IN THIS SAMPLE PRESENTATION: "ENCODE SANS" FOR TITLES AND "OPEN SANS" FOR BODY TEXT - These can be downloaded and installed on your computer for free here: <https://www.washington.edu/brand/graphic-elements/font-download/>



STUDENTS: DOUGLAS SMITH, DUSTIN WERRAN, JANE DOE

The Large Hardon Collider

- The Large Hadron Collider (LHC) is the largest particle collider in the world. Physicists are interested in observing rare events by colliding two high energy particle beams.
- An upcoming upgrade to the detector will substantially increase the amount of collisions per second.
- New technologies are being developed to cope with the substantial increase in particle flux.

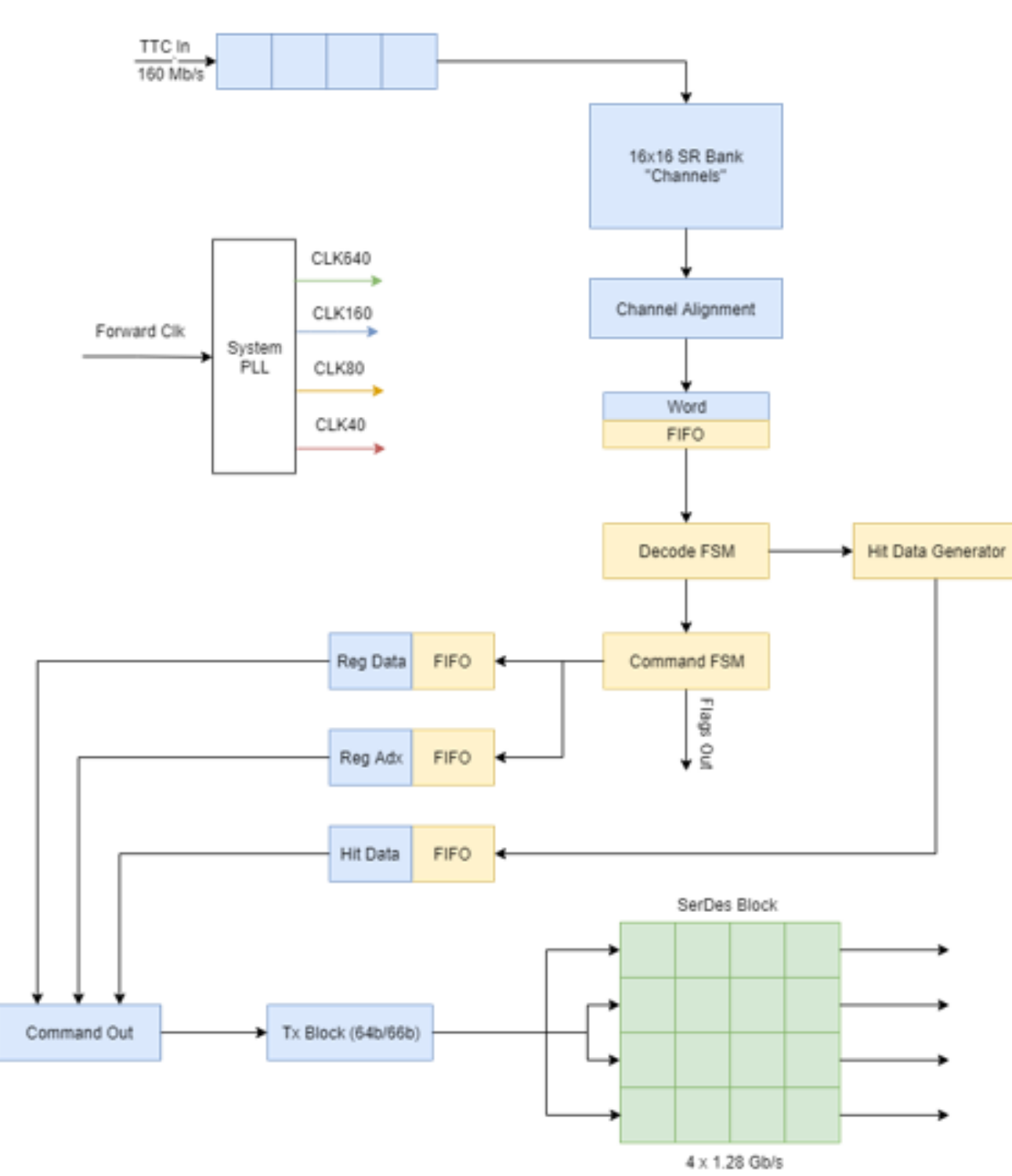
RD53A Emulator

- ACME Lab is developing an FPGA emulator of the LHC RD53A chip.
- The Emulator is able to recreate accurate hit signatures without actually being exposed to radiation, greatly simplifying its use.
- The emulator can be used for stress testing and can easily be reconfigured to target specific test cases.



Emulator Features

- Input data is received at 160 MBPS and is decoded using the custom RD53A protocol.
- The received data is split into system commands and triggers (requests for hit data) and each is sent to their respective response units.
- Commands are decoded and processed into appropriate system behavior such as rd-reg or wr-reg.
- Triggers are processed and produce hit data.
- Command and trigger output are combined into one data stream.
- This data is split over four lanes and is encoded using Aurora 64/66B at 640 Mbps.

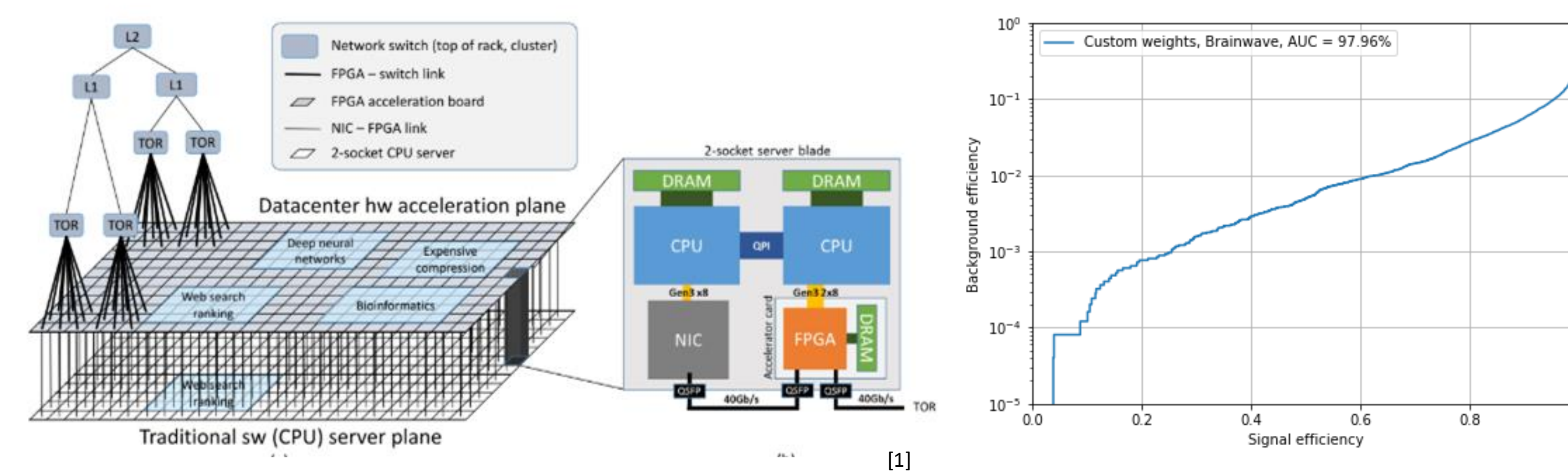


Machine Learning Acceleration for HEP

- Machine Learning is a popular solution to HEP issues, like hit tagging.
- However, ML needs hardware acceleration to be effective at large scale.
- ACME Lab is working with CMS at Fermilab to make machine learning acceleration accessible to the HEP community.

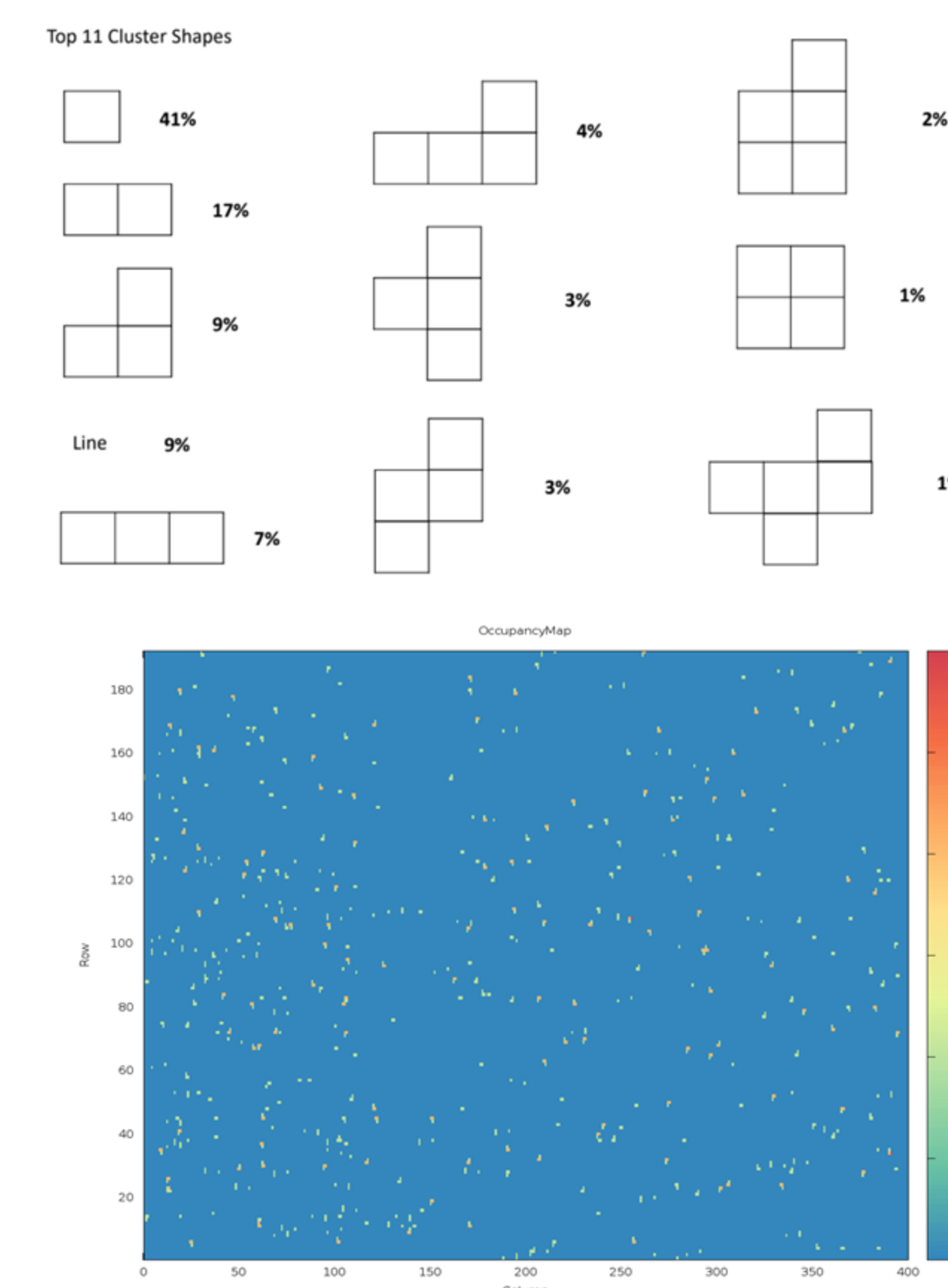
ML Acceleration in the Cloud

- Microsoft provides a cloud service called Brainwave, which applies FPGAs to the task of machine learning acceleration.
- We are doing research into the efficacy of Brainwave for HEP applications.
- Results look promising in the area of Top quark tagging.



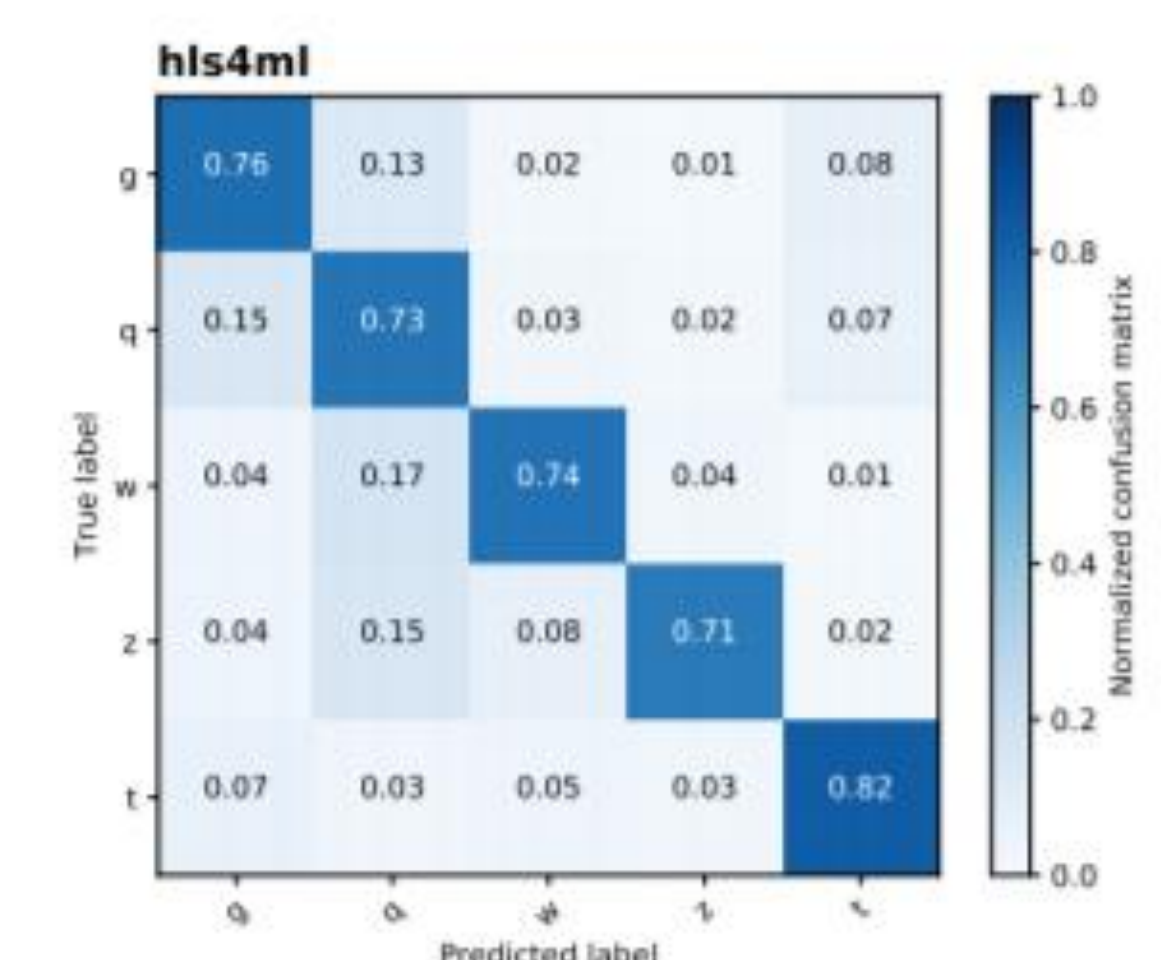
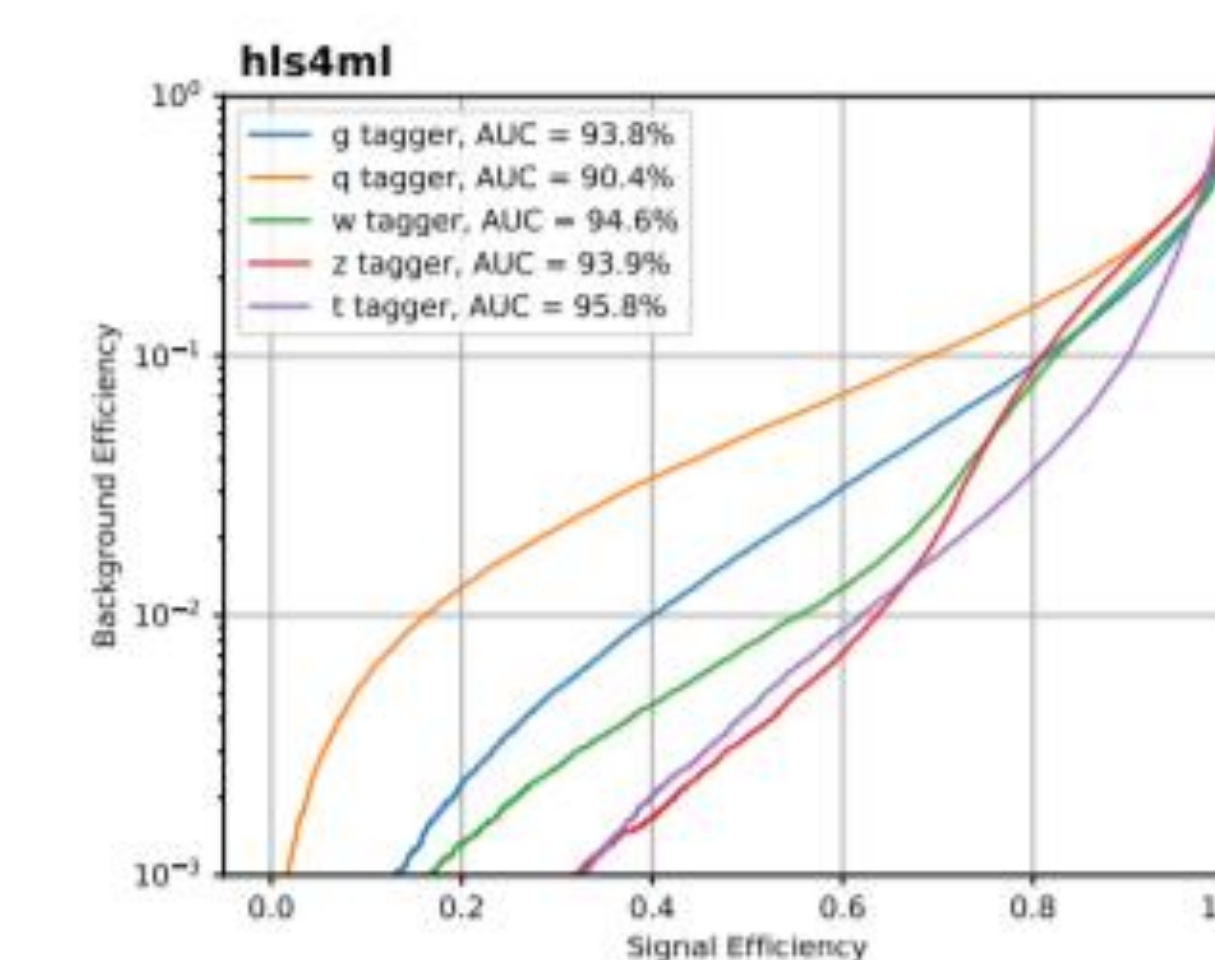
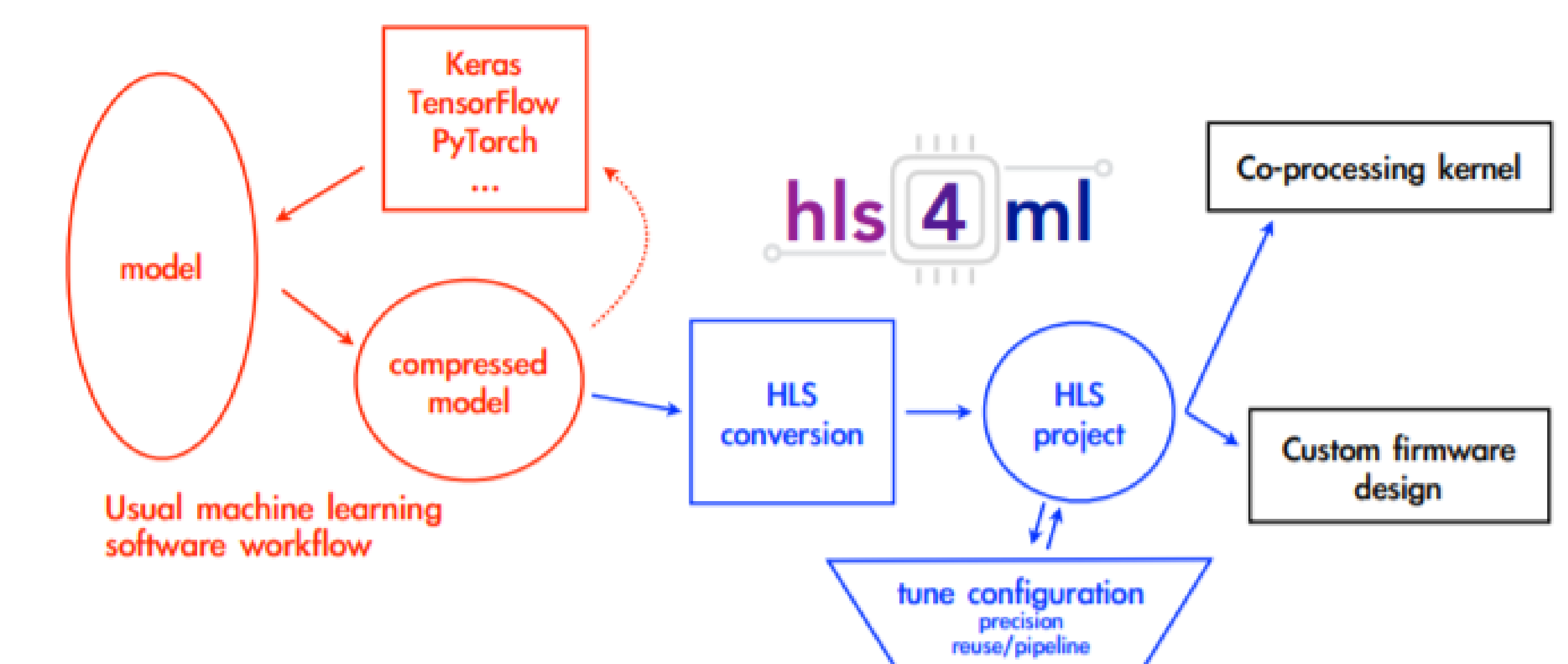
Hit Data/ Hit Generator

- One of our main goals in the RD53A project is to produce realistic data that matches what would be seen in the LHC.
- To determine what our data should look like we have been using image processing techniques to analyze real data from the LHC.
- Our testing has shown that most of the data consists of simple shapes and lines.
- Data is pseudo-randomly generated and output from the system via the Aurora lanes described to the right.
- A sample image to the right shows a generated hit patterning.
- To determine what our data should look like we have been using image processing techniques to analyze real data from the LHC.



Hls4ml

- FPGAs are a leading candidate for ML acceleration going forward. However, they require specialized knowledge to use.
- hls4ml is a tool that takes standard Neural Framework representations of DNNs and compiles them for use on FPGAs without requiring deep knowledge of FPGAs.



Current neural architectures under development:

- Fully Connected
- Convolutional NN

Current Framework support under development:

- TensorFlow
- Keras

Future Work, References, and Acknowledgments

- Further improvements to hls4ml
- Scaling up of Brainwave
- Finish implementing the RD53A hit data generator
- Start planning the upgrade to RD53B, the next test chip

Faculty: Scott Hauck, Shih-Chieh Hsu
Graduate Students: Douglas Smith, Dustin Werran, Richa Rao
Undergraduate Students: Tony Faubert, Jessica Lan, Kylie Lim, Matthew Trahms, Donovan Erickson

[1] A. Caulfield, E. Chung, A. Putnam, H. Angepat, J. Fowers, M. Haselman et al., A cloud-scale acceleration architecture, IEEE Computer Society, October, 2016.

[2] J. Duarte et al., Fast inference of deep neural networks in FPGAs for particle physics, arXiv:1804.06913v3 [physics.ins-det] 28